



CPS Creative Lab

Alghero, September 21st, 2026

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CEIMM

CENTRO DE ELECTRÓNICA INDUSTRIAL Y SISTEMAS MULTIMODALES



POLITÉCNICA

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DI SASSARI

Claudio Rubattu



Center for Industrial Electronics and Multimodal Systems (CEIMM)



CEIMM is a research center affiliated to the Universidad Politécnica de Madrid (UPM)

- UPM is the largest technical university in Spain and also the first in terms of employability.
- Number 73 in engineering and technology according to *QS World University Ranking*.
- UPM is also the first Spanish university in the obtention of external resources for R&D&I.
- CEI is the UPM research center specializing in power electronics and **digital embedded systems**.



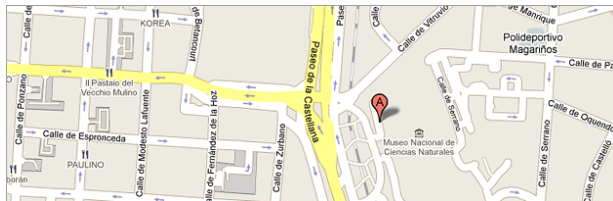
POLITÉCNICA



INDUSTRIALES
ETSII | UPM



Located in the City Center of Madrid



Biomedical Applications

Power Electronics

Acoustics & Multimedia

Digital Embedded Systems

Some Numbers

- 60 Full-time researchers
 - 26 Doctors (Faculty, Contracted researchers)
 - 21 Doctoral Students
 - 13 Researchers
- 50 Part-time, sponsored students (BSc & MSc)
- 4 Administration & Technicians

Members of :



The Creative Lab at CPS 2026

The Creative Lab is a **highly practical hands-on experience** meant to promote the exchange of ideas between PhD students and young researchers with the spirit of creating a new business culture.

This year's topic:

Smart cyber-physical edge systems

Learning by doing!



What is Reconfigurable Computing?

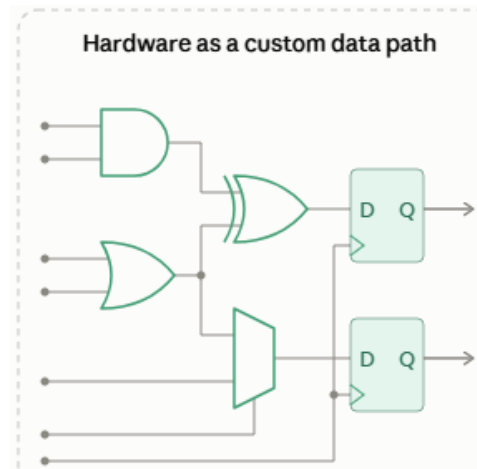
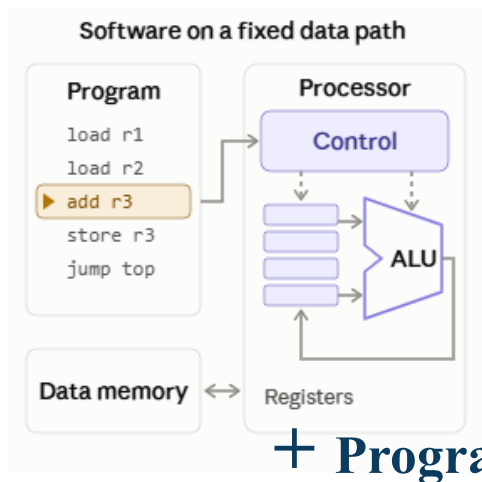


WIKIPEDIA
The Free Encyclopedia

Reconfigurable Computing is a computer architecture combining some of the **flexibility** of software with the **high performance** of hardware by processing with very flexible high speed computing fabrics like field-programmable gate arrays (FPGAs). The principal difference when compared to using microprocessors is **the ability to make substantial changes to the data-path** itself in addition to the control flow.

Fixed Datapath

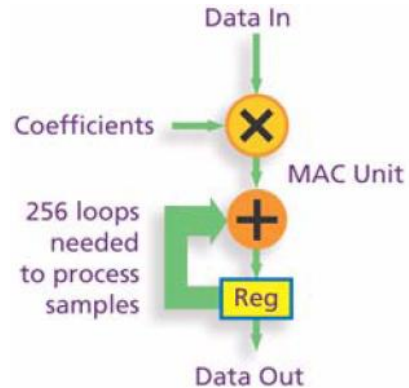
Custom Computing



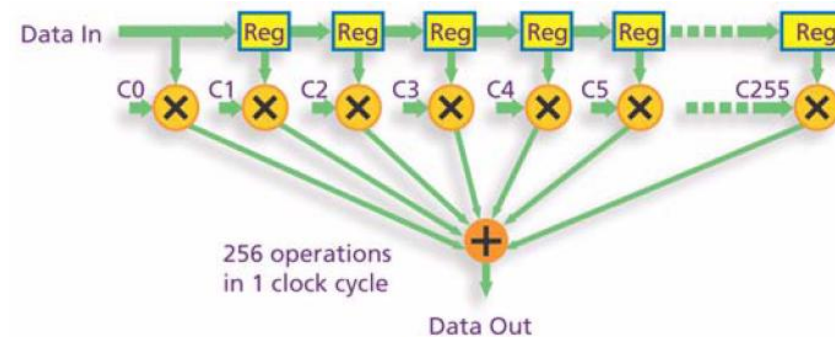
Parallel Processing and Custom Computing

Consider a convolution filter...
$$Y_{(n)} = \sum_{i=0}^{i=N-1} k_i \cdot X_{(n-i)}$$

Sequential Implementation (Temporal Decomposition)



Parallel Implementation (Spatial Distribution)

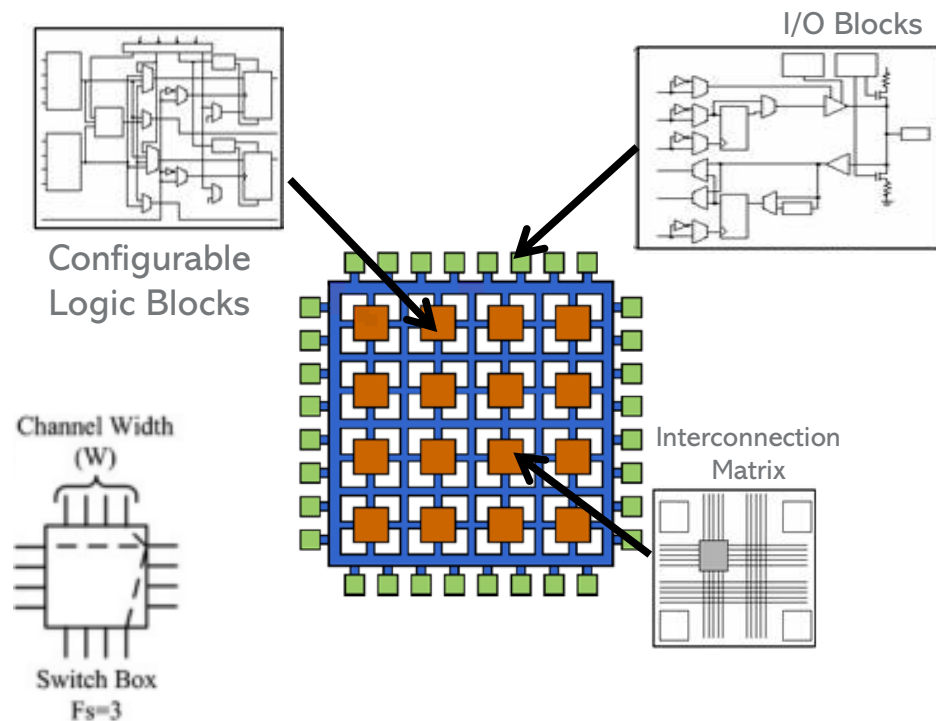


General Purpose Architectures are able to do everything



FPGA Architectures

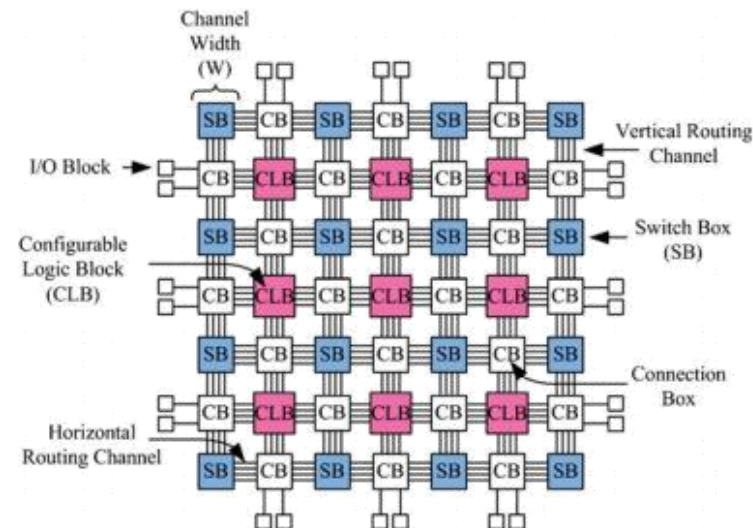
FPGAs are fine grain reconfigurable devices composed by logic elements with a functionality that can be modified as many times as needed.



CLB: Configurable Logic Block

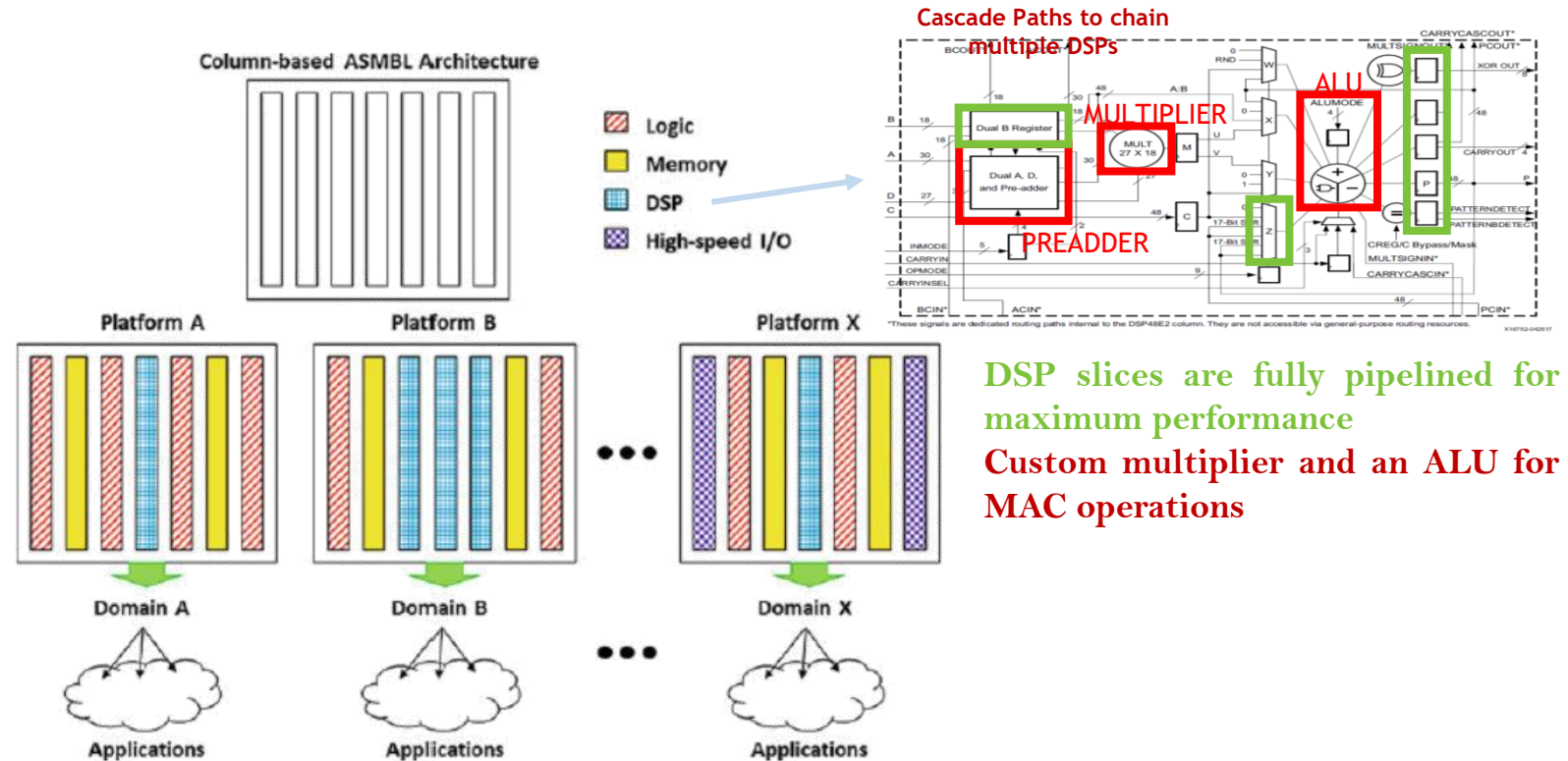
CB: Connection Box

SB: Switch Box or Switch Matrix

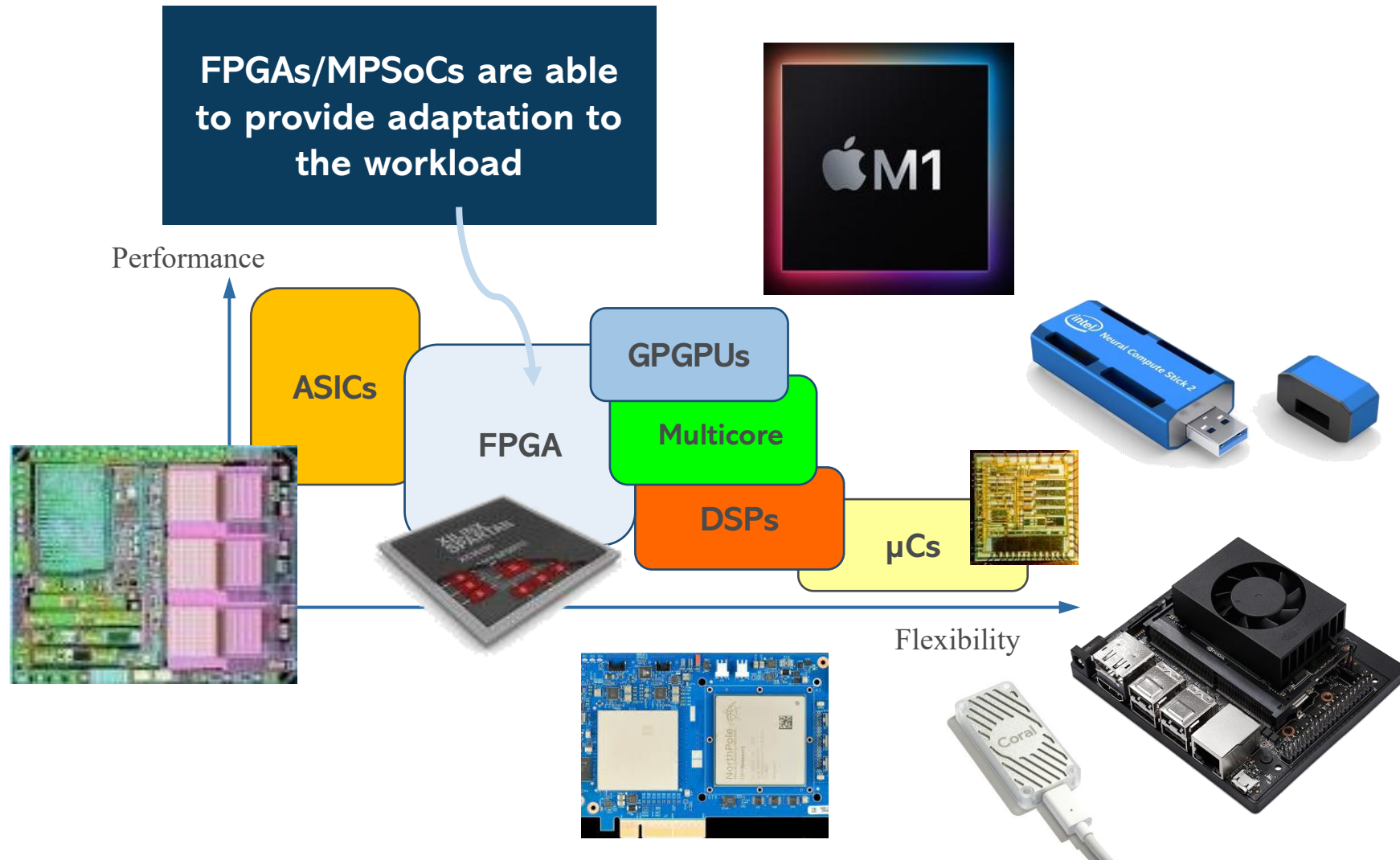


FPGA Architecture: Heterogeneous Arrays

- To increase performance and flexibility, some reconfigurable devices have a layout with embedded heterogeneous resources, such as:
 - Custom DSP function blocks
 - Memory blocks to store frequently used data and variables on-chip for quick access, thanks to the proximity to the logic blocks that access it.

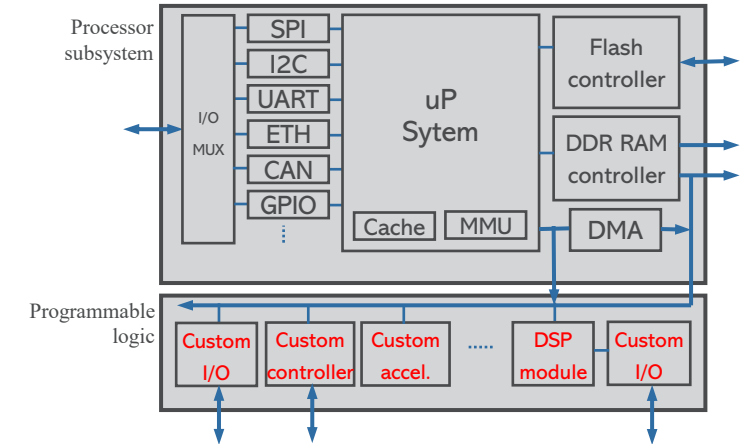


FPGAs for AI Acceleration



Mixed Software / Hardware Systems

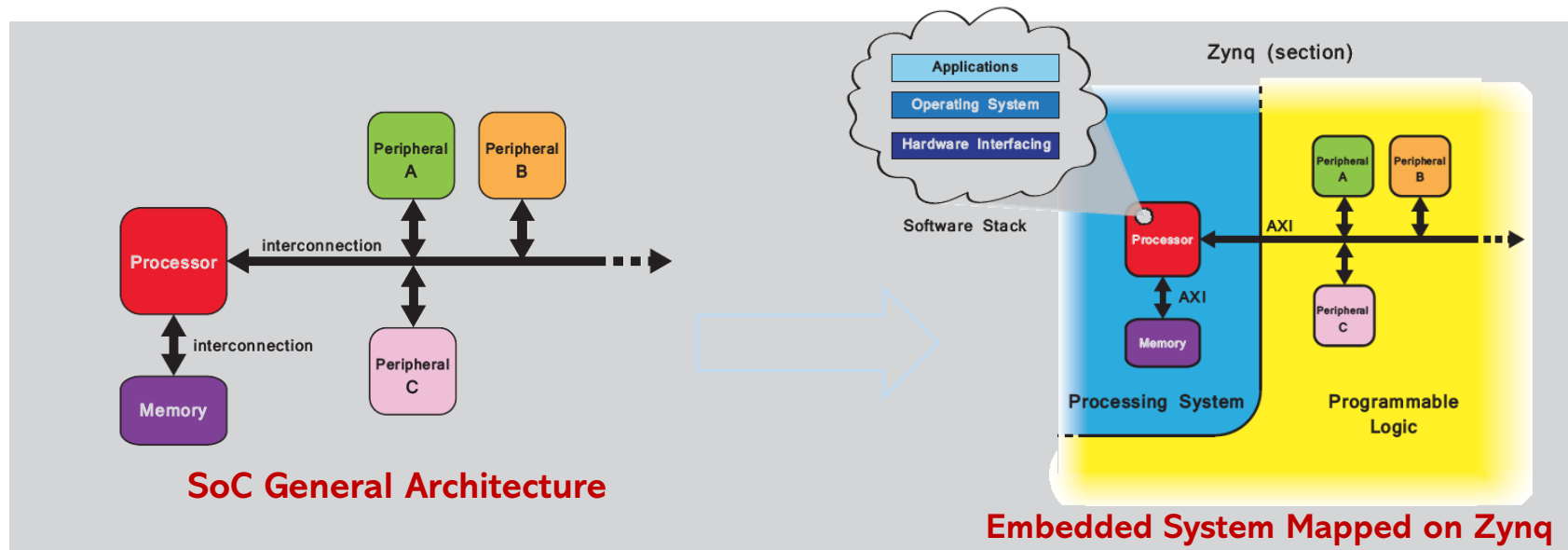
- Best-of-both-worlds approach
 - Microprocessor(s) for sequential application execution
 - FPGA logic for massively parallel computation
- Different approaches
 - Traditional: System on Programmable Chip (SoPC)
 - Microprocessors embedded in FPGA logic
 - Hard cores: silicon with fixed functionality (PowerPC)
 - Soft cores: implemented using FPGA logic resources (MicroBlaze, Nios II)
 - Current: System on Chip (SoC) + FPGA
 - Silicon is split in ASIC-like CGRA and FPGA parts
 - Microprocessors can operate without enabling the FPGA



System-on-Programmable Chips (SoPCs)

System-on-Programmable-Chips (SoPCs)

Architectural concept resulting from the integration of 'hard' CPU cores with an FPGA in the same chip



“The **PL** section is ideal for implementing high-speed logic, arithmetic and data flow subsystems, while the **PS** supports software routines and/or operating systems“
(from *The Zynq Book*)



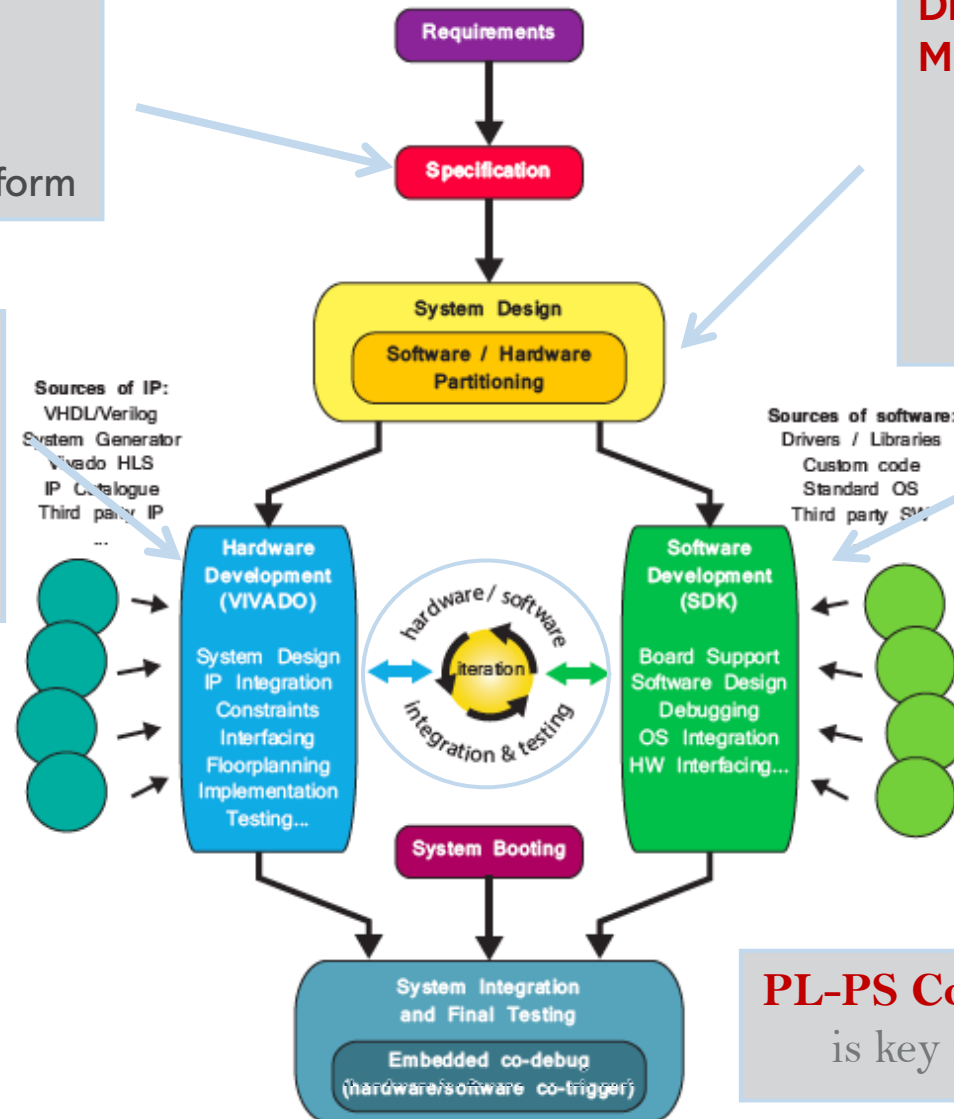
SoC Based Design for Zynq (Vivado & SDK)

Functionality
Interfaces
Performance Criteria
Target Device or Platform

PL: Computational Intensive Dataflow
Coprocessor model
Which tasks can be parallelized?

DESIGN ENTRY METHODS

VHDL, Verilog
System Verilog
C, C++
System C
Matlab
Simulink



PS: SEQUENTIAL PROCESSING TASKS

Operating System?
User Application
GUI
Networking?

PL-PS Communication latency
is key for the performance

Creative Lab Components: AMD-Xilinx Kria KV260

Kria™ KV260 Vision AI Starter Kit

VISION READY

- Multi-Camera Support: Up to 8 interfaces
- 3 MIPI sensor interfaces, USB cameras
- Built-in ISP component
- HDMI, DisplayPort outputs

FLEXIBLE CONNECTIVITY

- 1Gb Ethernet
- USB 3.0 / 2.0

EXPANDABLE

- Extend to any sensor or interface
- Access Pmod ecosystem

ACCESSIBLE

- Low cost, enabling design exploration
- Available from Xilinx and distributors

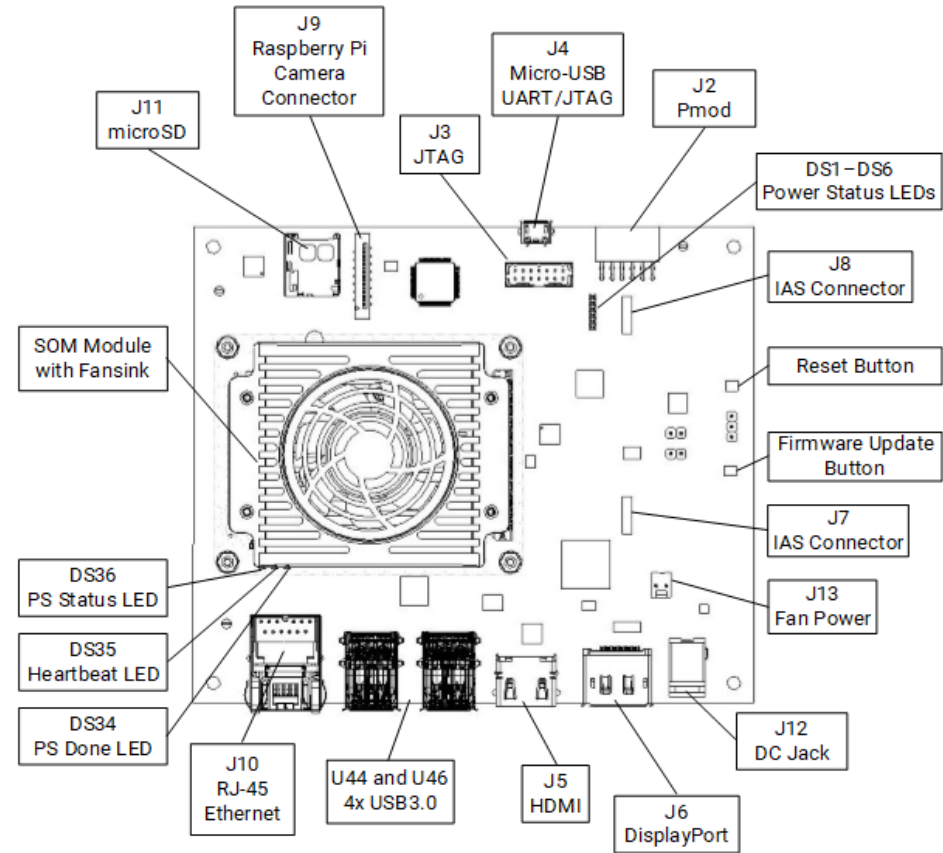
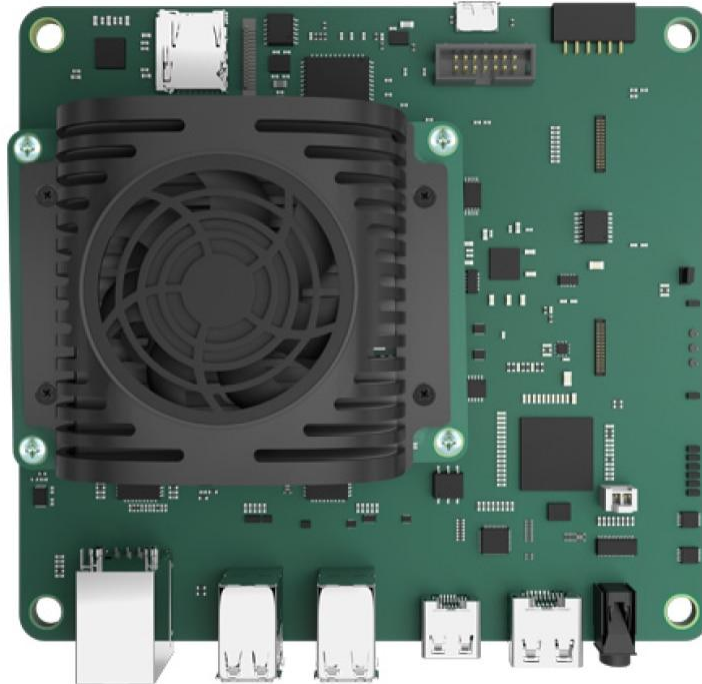


Creative Lab Components: AMD-Xilinx Kria KV260



Creative Lab Components: AMD-Xilinx Kria KV260

Kria™ KV260 Vision AI Starter Kit



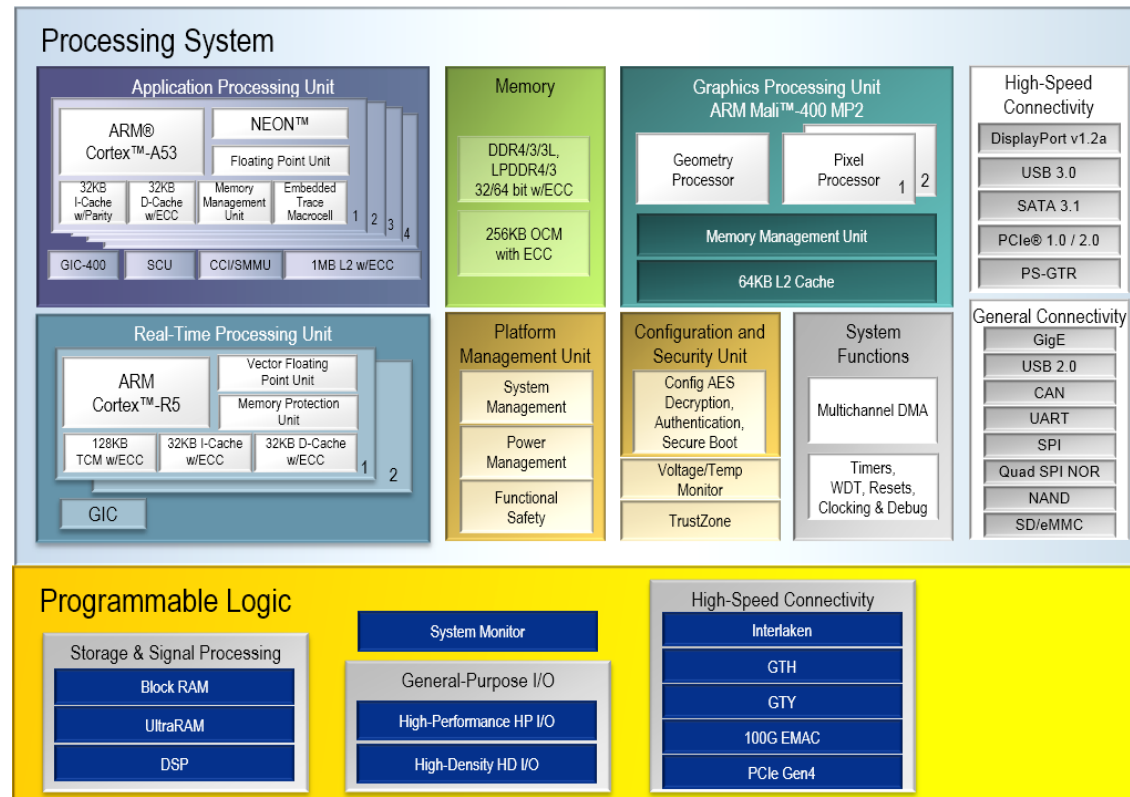
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Creative Lab Components: AMD-Xilinx Kria KV260

■ Zynq UltraScale+ EG

- Quad-core ARM® Cortex-A53 processors @1.5GHz
- 16nm FinFET+ FPGA
- Dual-core Cortex-R5 real-time processors
- Mali-400 MP2 GPU

Xilinx Zynq
UltraScale+ MPSoC



How to reach the board?

Open the terminal:

```
$ dmesg | grep tty
```

```
$ sudo putty /dev/ttyUSBXXXX -serial -sercfg  
115200,8,n,1,N
```

```
$ ip a
```

```
usr:pwd → ubuntu:alghero24
```

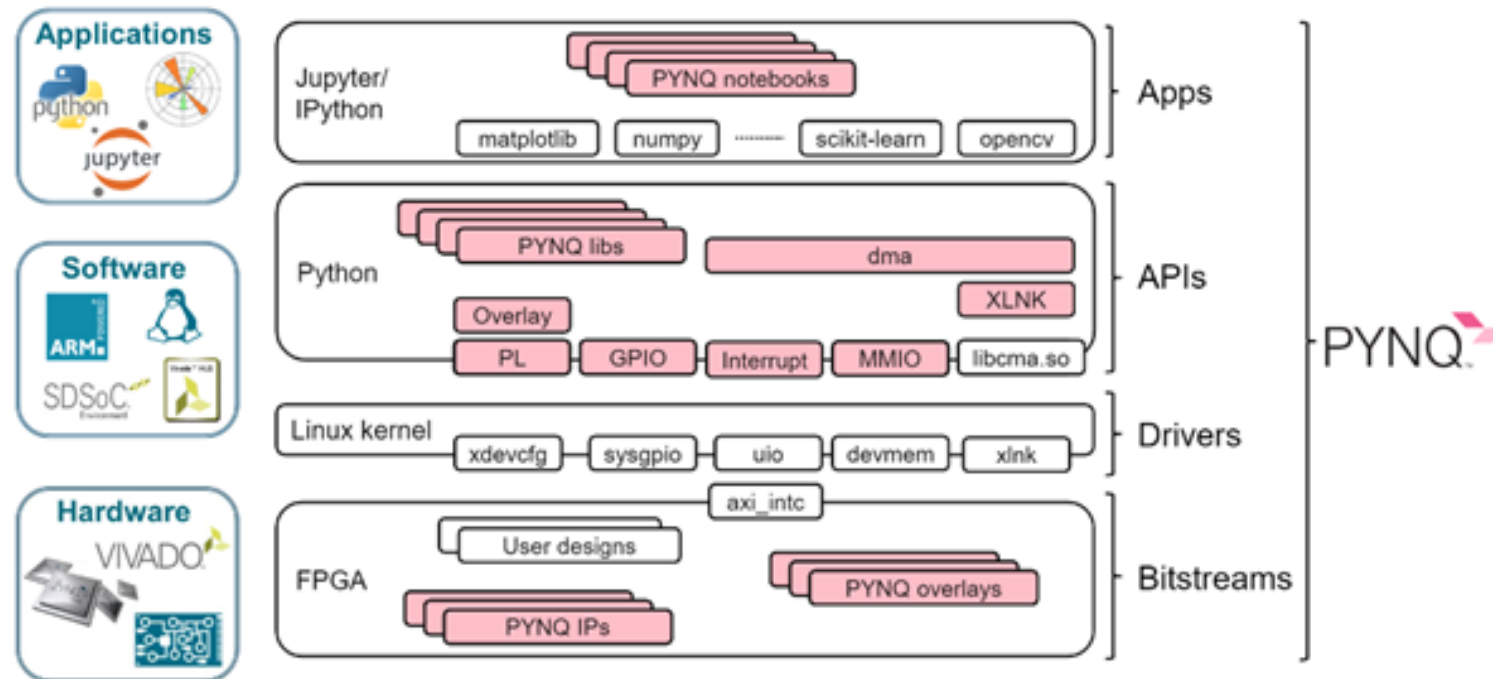
via SSH (discover ip first)

```
$ ssh ubuntu@<my_magic_ip>
```



Creative Lab Components: The PYNQ Framework (I)

PYNQ is an open-source project started by Xilinx, which fuses the productivity of Python with the acceleration provided by programmable logic within the Zynq / Zynq MPSoC.



Creative Lab Components: The PYNQ Framework (II)

As developers, we leverage the PYNQ framework by connecting to the Jupyter server over a wired ethernet link and developing our application in a browser-based interface.



Now you can access **JupyterLab** via browser:
<ip_address>:9090/lab or

The password is: **xilinx**

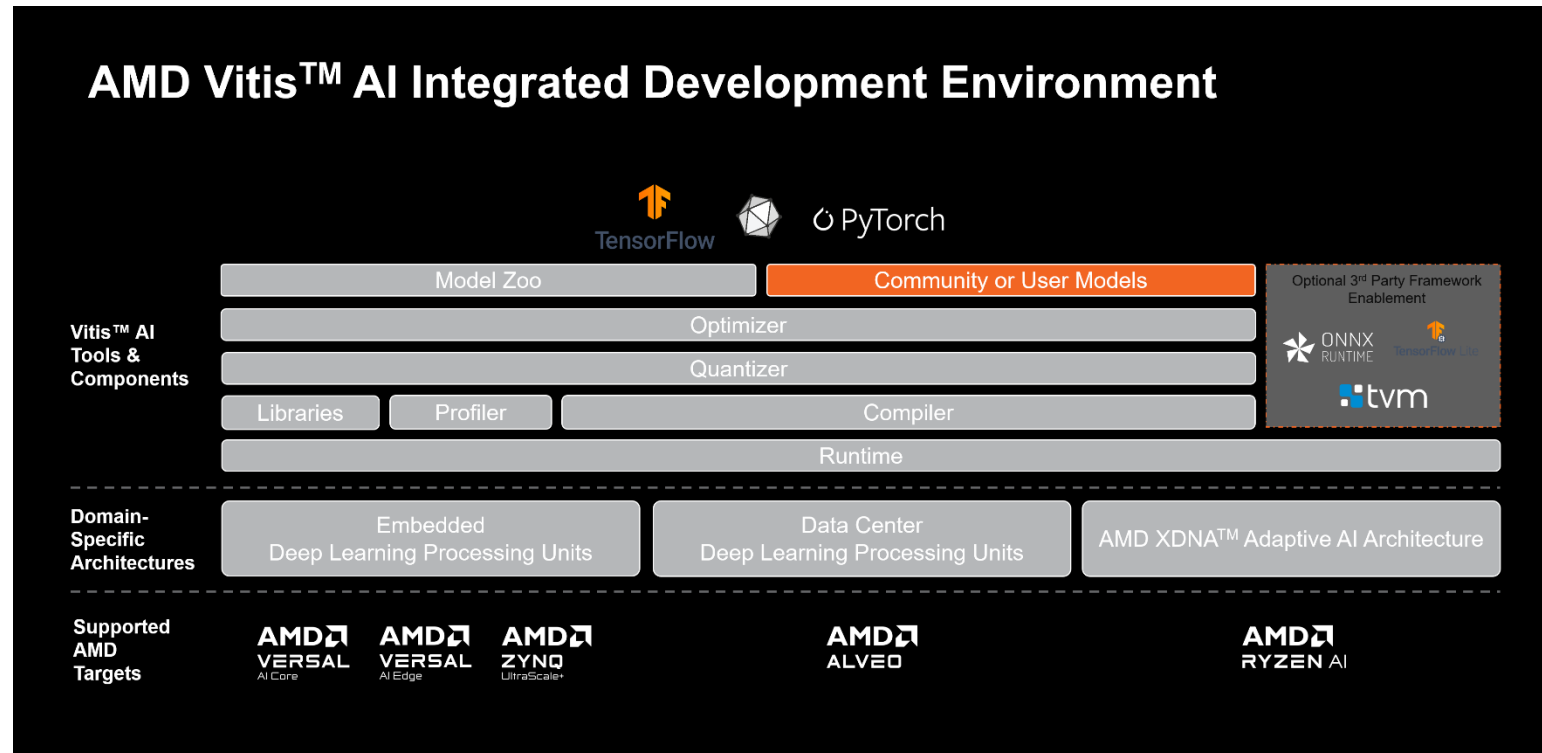


Creative Lab Components: The PYNQ Framework (II)

- Community overlays — what overlays are available for our PYNQ applications?
- Creating applications using available overlays, e.g. image processing, BNN, etc.
- Creation of our own overlays — how do we make a simple overlay from scratch?
- Custom PYNQ images — how do we build and deploy PYNQ images for custom boards? PYNQ images can be generated for both Zynq and Zynq MPSoC-based boards.

Creative Lab Components: Vitis AI

Adaptable & Real-Time AI Inference Acceleration



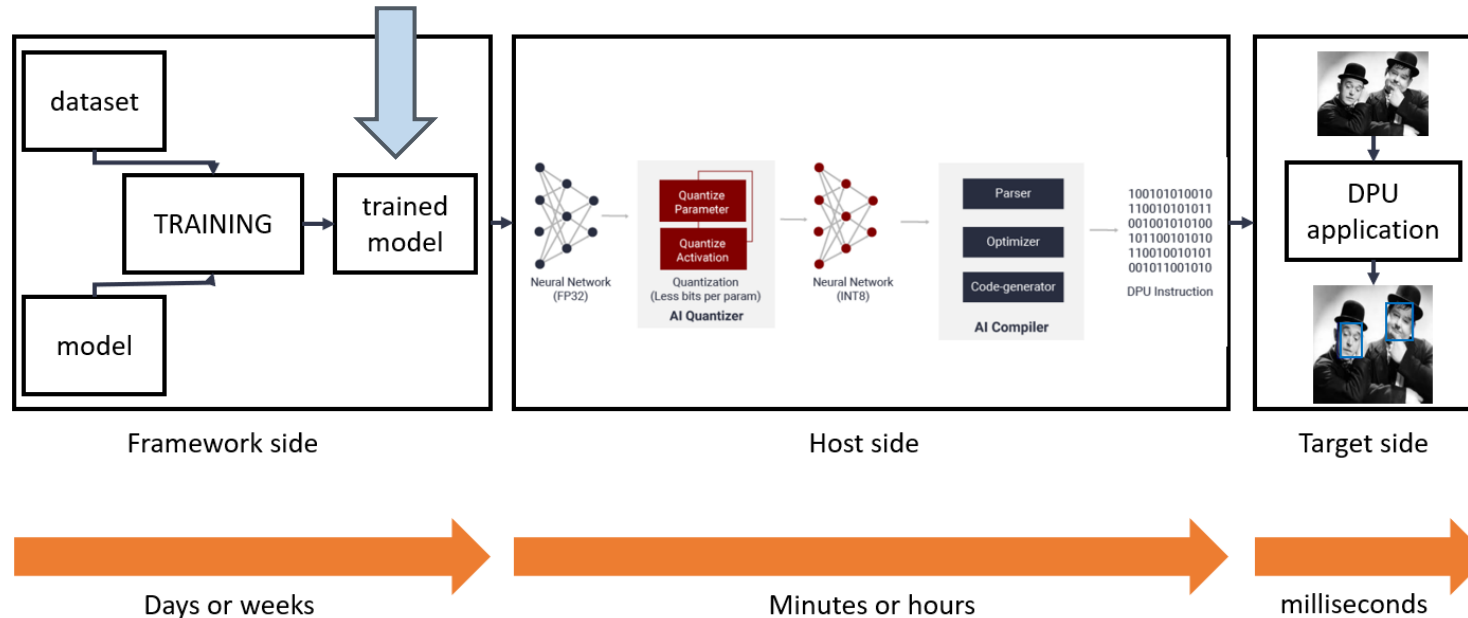
<https://github.com/Xilinx/Vitis-AI>



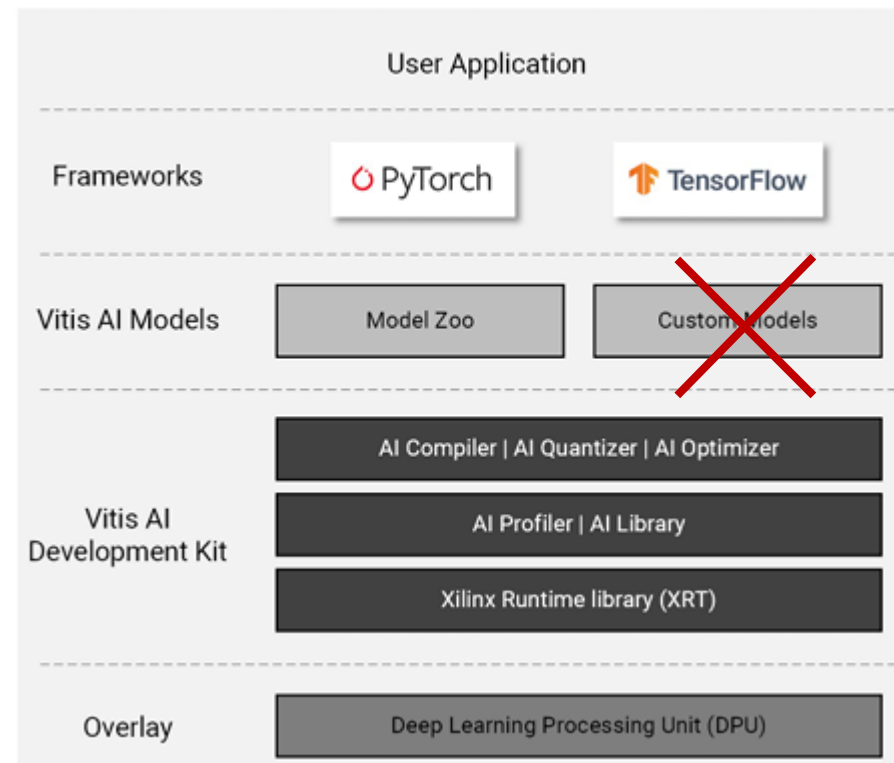
Creative Lab Components: Vitis AI



Entering here for the creative lab

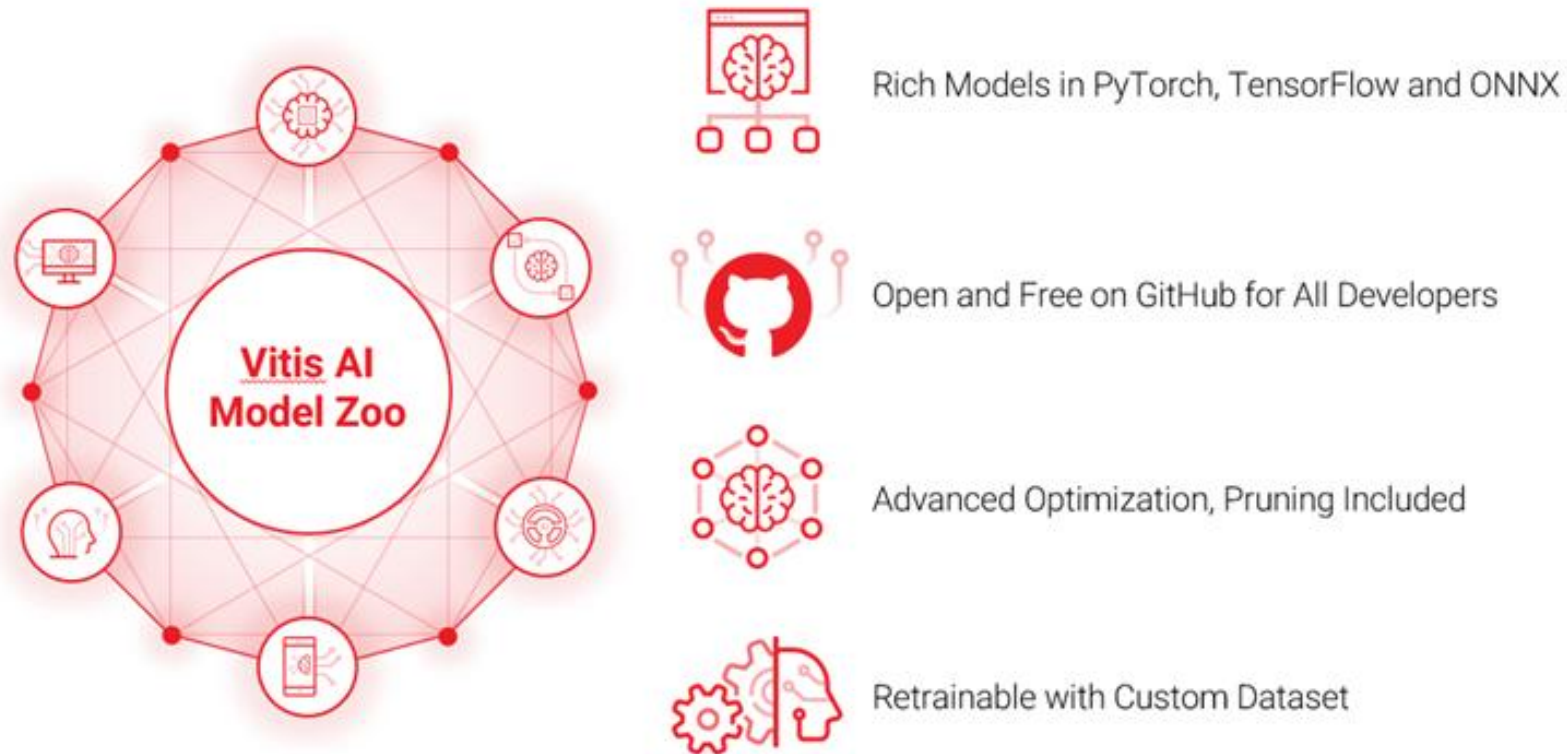


Creative Lab Components: Vitis AI



Vitis AI Model Zoo

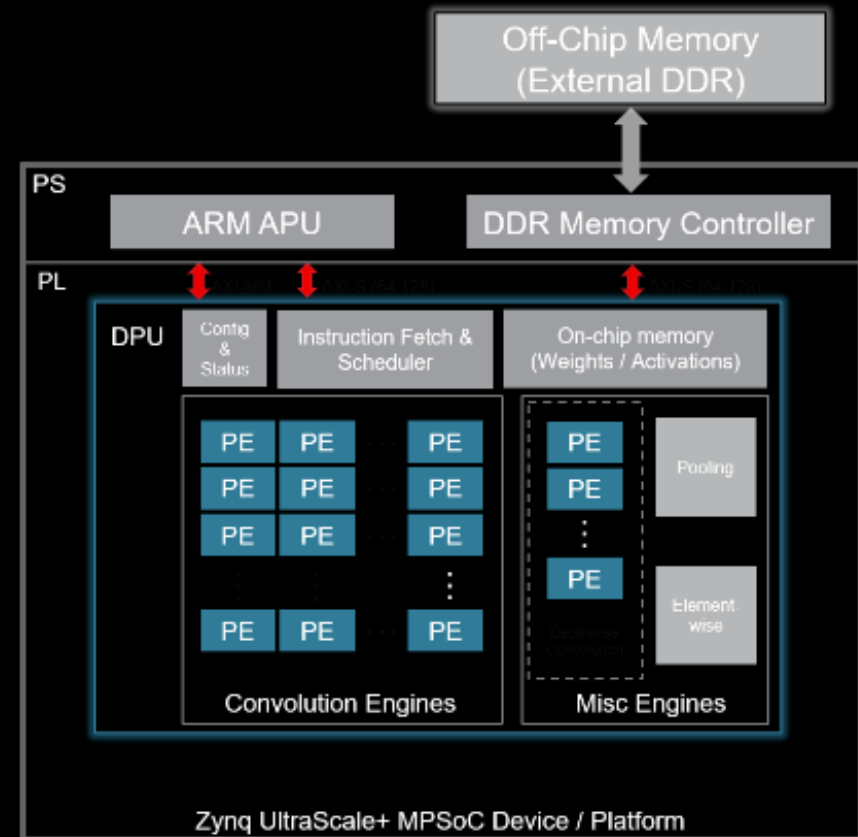
<https://github.com/Xilinx/AI-Model-Zoo/>



Creative Lab Components: DPU & run-time

DPU for the Zynq® UltraScale+™ MPSoC

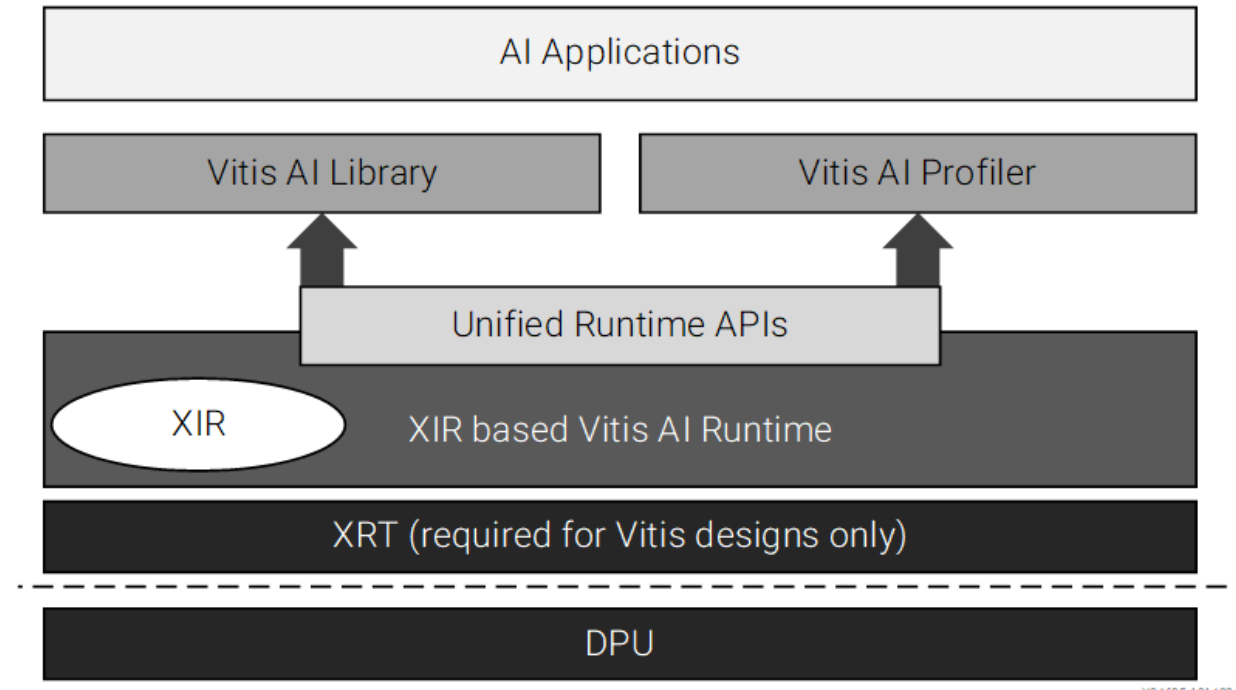
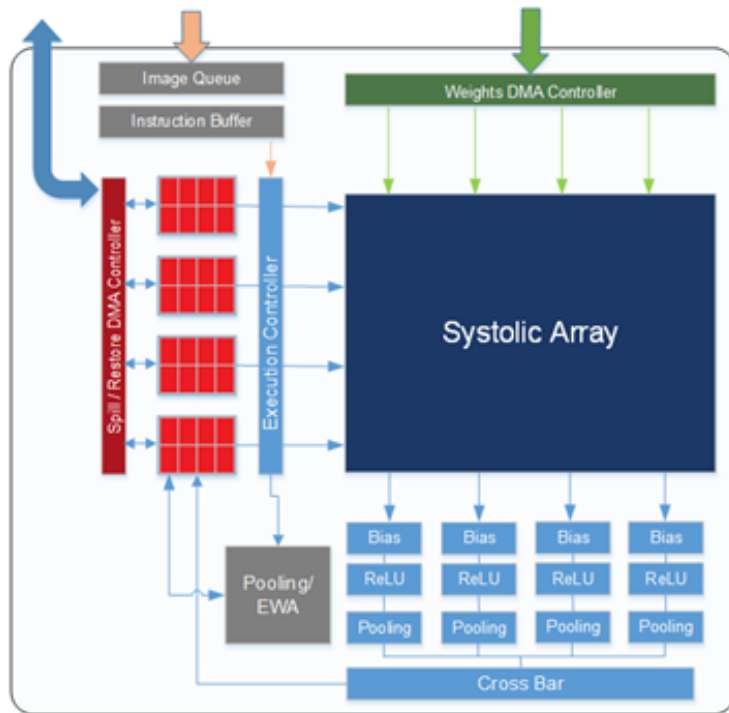
- “**Deep learning Processing Unit**”
 - “Matrix of Processing Engines” (MPE) architecture
 - Composed of DSPs, LUT, FFs, BRAM, UltraRAM (optional)
 - Soft-logic, micro-coded processor for INT8 deep learning inference
 - Graph compiled as micro-code, executed on DPU
 - Operator fusion, INT8 quantization, weights shuffled for optimized performance
 - Linux, QNX, and Integrity runtime enablement (QNX / Integrity support as POC, beta)
- Dedicated data movers and AXI stream interfaces for:
 - Instruction fetch
 - Weight and activation load/store
- Dedicated AXI memory-map interface for DPU configuration and status register access
- Global memory pool for buffering of intermediate activations
 - Optimizes and minimizes DDR bandwidth requirements
- Scalable from low to high parallelism (OPs)
 - 1 to 4 DPU cores per target device
 - Size DPU parallelism to fit available logic
 - Configurations for low / high DSP, RAM utilization, UltraRAM



<https://github.com/Xilinx/DPU-PYNQ>



Creative Lab Components: DPU & run-time



X24605-121422

<https://github.com/Xilinx/DPU-PYNQ>

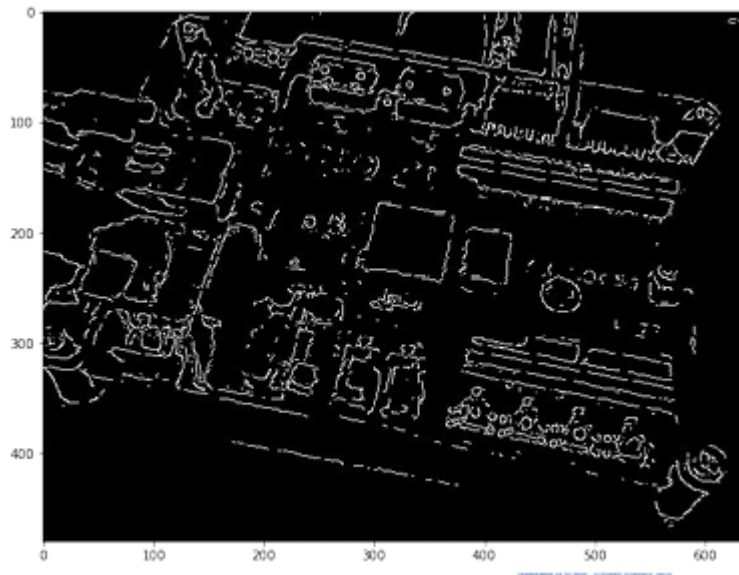


Creative Lab Scheduling 2024

Monday		Tuesday		Wednesday		Thursday		Friday	
<i>Introduction</i>		<i>Open-</i>		<i>Modelling and Design at the edge</i>		<i>Data Analysis and Security</i>		<i>Creative Lab Day</i>	
8:15-8:30	Registration								
8:30-9:00	School and Day Opening	8:50-9:00	Opening	8:50-9:00	Opening	8:50-9:00	Opening	8:50-9:00	Opening
9:00-10:30	Ayşe Coskun (Boston University and Emerald AI)	9:00-10:30	Lana Josipović (ETH Zurich)	9:00-10:30	Jerónimo Castrillón Mazo (TU Dresden)	9:00-10:30	Andrés Otero and Alfonso Rodríguez (Universidad Politécnica de Madrid)	9:00-10:30	Creative Lab @ work
10:30-11:00	Break	10:30-11:00	Break	10:30-11:00	Break	10:30-11:00	Break	10:30-11:00	Break
11:00-12:30	Alberto Sangiovanni-Vincentelli (UC Berkley)	11:00-12:30	Quantum Tutorial (EPFL Lausanne)	11:00-12:30	MLIR Tutorial from the MYRTUS Project	11:00-12:30	Security Tutorial from the SECURED Project	11:00-13:00	Creative Lab @ work
12:30-13:15	Creative Lab Presentation	12:30-13:00	Creative Lab @ work	12:30-13:00	Paolo Azzoni (INSIDE Industry Association)	12:30-13:00	Creative Lab @ work		
13:15-14:15	Lunch	13:00-14:00	Lunch	13:00-14:00	Lunch	13:00-14:00	Lunch	13:00-14:00	Lunch
14:15-16:00	CPS Workshop	14:00-15:30	Ingrid Verbauwhede (KU Leuven)	14:00-15:30	Theo Theocharides (University of Cyprus)	14:00-15:30	Battista Biggio (University of Cagliari)	14:00-15:30	Creative Lab Pitch and Demo (5min pitch+10min demo+5min questions)
		15:30-As needed	Creative Lab @ work	15:30-As needed	Creative Lab @ work	15:30-17:00	Tutorial on Testing Adversarial Robustness of Document Analysis Systems (University of Cagliari)	15:30-16:00	Creative Evaluation Meeting
								16:00-16:30	Creative Lab & School Closing Session

A Demo

- AMD Demo based on USB Camera acquisition



<https://xilinx.github.io/kria-apps-docs/kv260/2022.1/build/html/index.html>

https://github.com/Xilinx/PYNQ/blob/master/boards/Pynq-Z1/base/notebooks/video/opencv_filters_webcam.ipynb





Creative Lab Teams

Creative Lab Teams

■ Red Team

- Tauseef Ahmed
- Malte Kerl
- Federico Manca
- Viviane Potocnik

■ Green Team

- Miloš Đorđević
- Mohammad Cheshfar
- Andrea Magnani
- Andreas Vasiliou



Creative Lab Teams

■ Blue Team

- Gianluca Bellocchi
- Kai Berszin
- Fabio Cabeccia
- Franziska Sievert

■ Orange Team

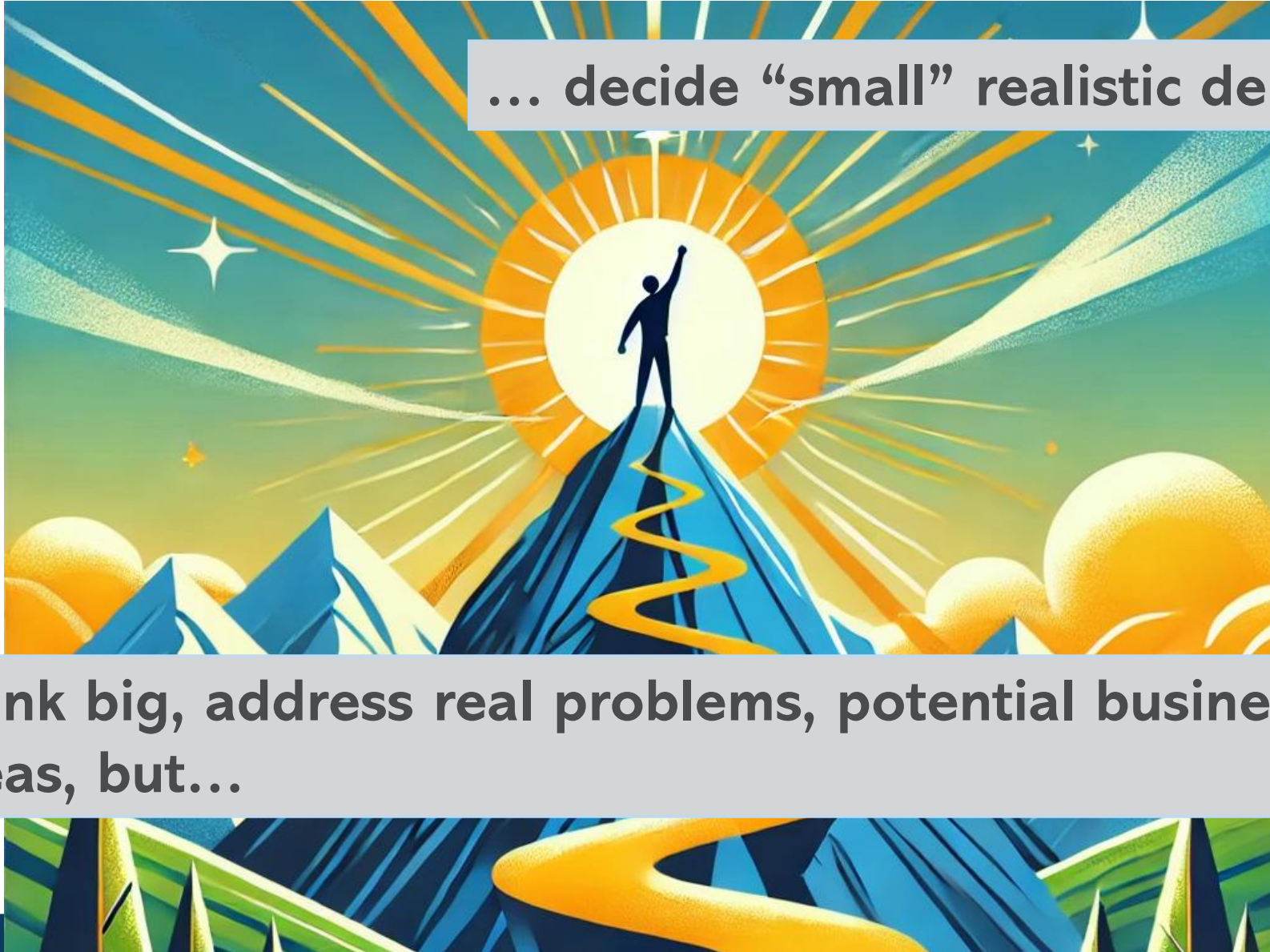
- Francesco Giulio Blanco
- Juan Gallego
- Raffaele Meloni
- Foteini Paraskevopoulou



“Good” Creative Lab Projects

... decide “small” realistic demos.

Think big, address real problems, potential business ideas, but...



Useful Links

Setting Up the Board and Application Deployment

https://xilinx.github.io/kria-apps-docs/kv260/2022.1/build/html/docs/smartcamera/docs/app_deployment.html

Ready to use notebooks:

<https://github.com/Xilinx/Kria-PYNQ/tree/main/kv260/base/notebooks/microblaze>

<https://github.com/Xilinx/Kria-PYNQ/tree/main/kv260/base/notebooks/video>

https://github.com/Xilinx/DPU-PYNQ/tree/master/pynq_dpu/notebooks

https://github.com/Xilinx/PYNQ_Composable_Pipeline

Model Zoo for PYNQ-DPU based models (2.5 Vitis AI):

https://github.com/Xilinx/Vitis-AI/tree/2.5/model_zoo

Vitis AI Library

<https://docs.xilinx.com/r/2.5-English/ug1354-xilinx-ai-sdk/Introduction>

Vitis AI User Guide v2.5

<https://docs.xilinx.com/r/2.5-English/ug1414-vitis-ai/Vitis-AI-Overview>

