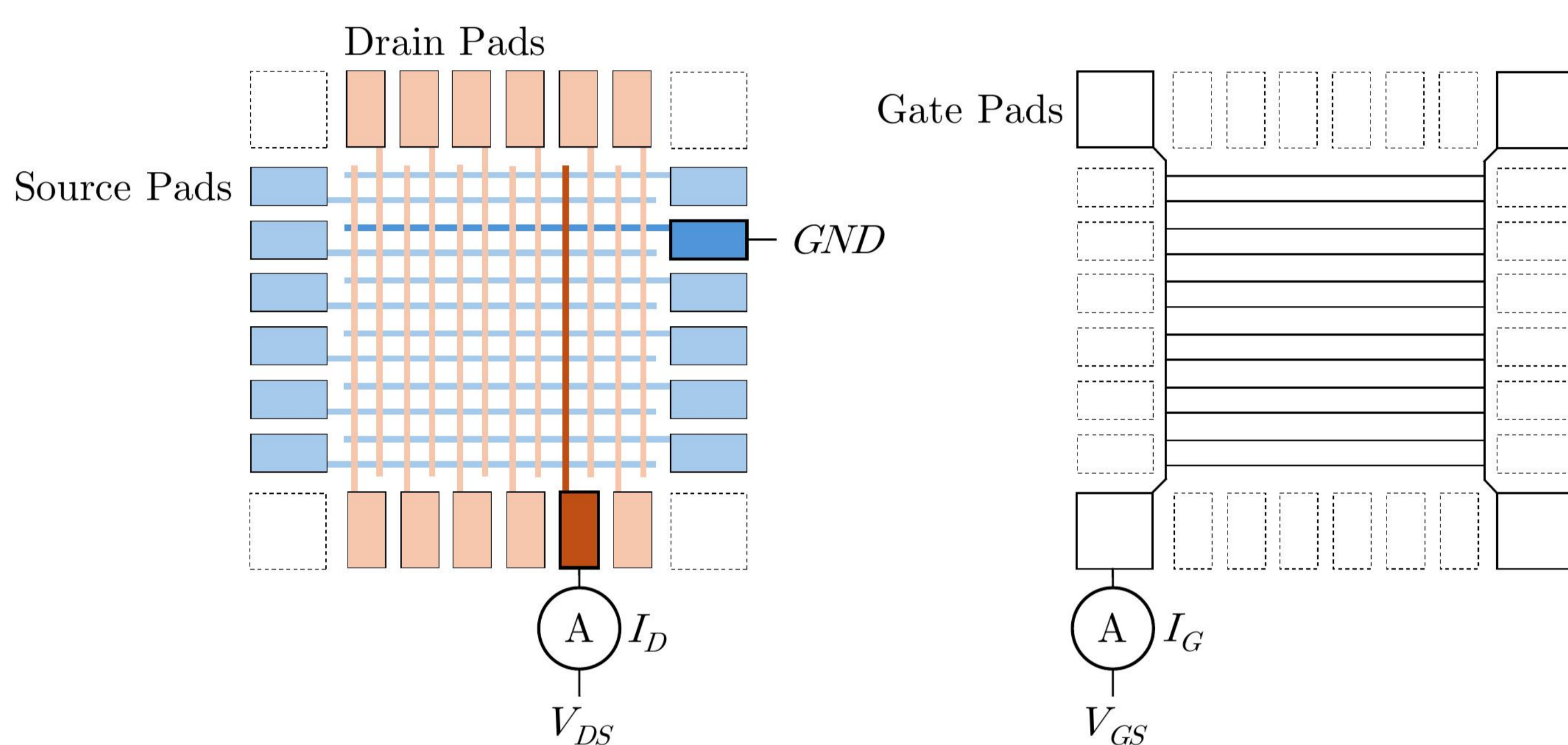


Towards the FPGA Platform Integration of Carbon-Nanotubes in Physical Unclonable Functions

Introduction

Motivation

- **Physical Unclonable Functions (PUFs):** Serves as a method for key storage, authentication and tamper-detection
- **CMOS-based PUFs Face Limitations:** Aging effects, sensitivity to temperature and voltage variations
- **Opportunity with Emerging Nanomaterials:** Materials explored for future technology nodes promise improved robustness for PUF implementations



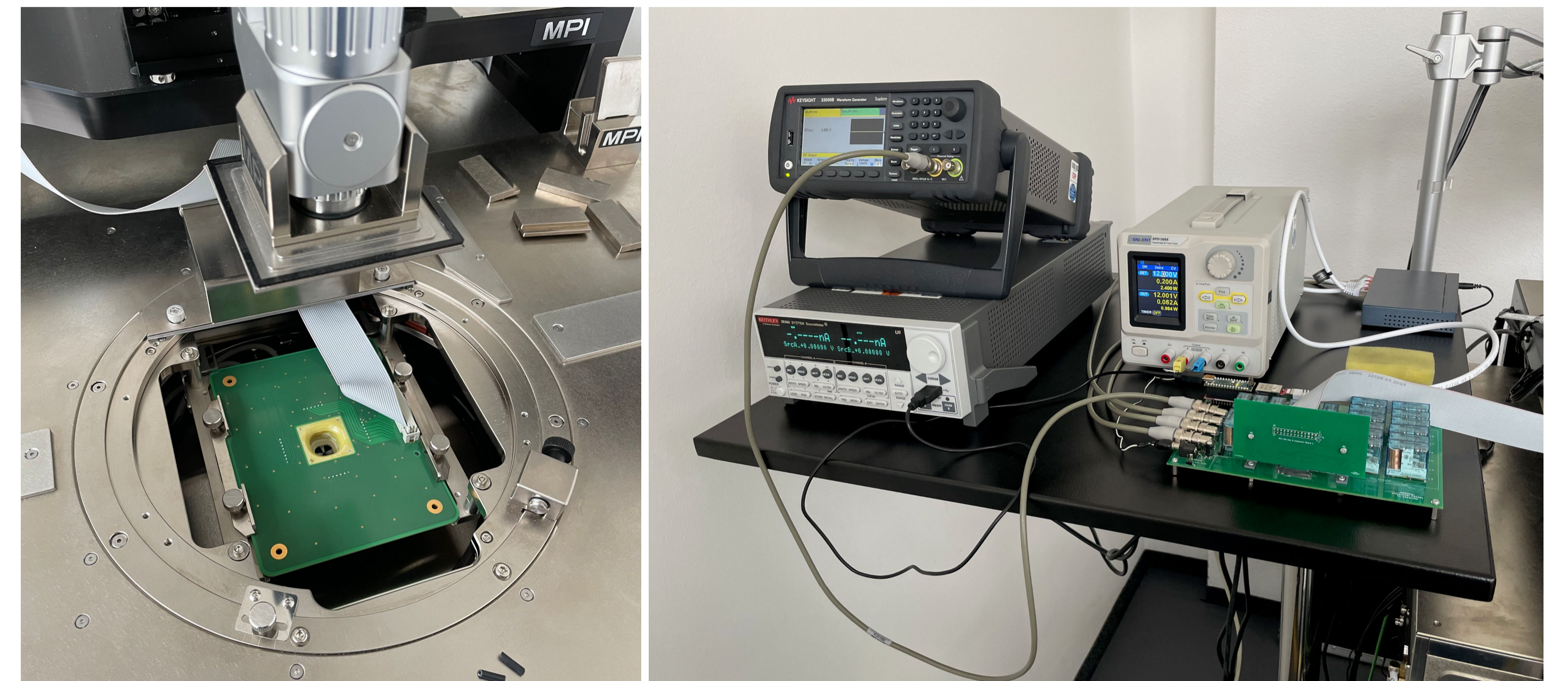
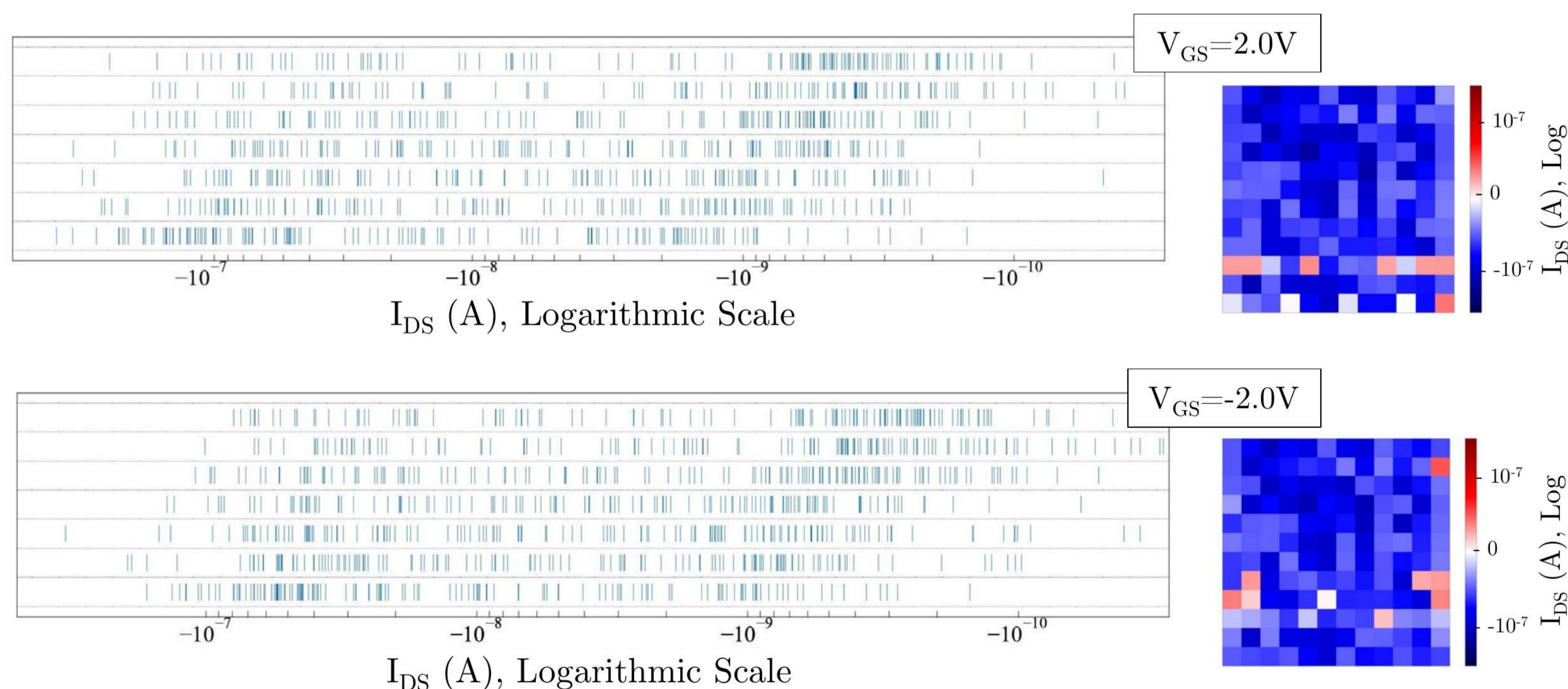
Concept and Challenges

- Build addressable 12x12 on-wafer crossbar arrays containing **carbon nanotube field-effect transistors (CNTFETs)**
- **PUF Principle:** Random alignment of CNTs in each CNTFET yields differently behaving cells (conductance, on/off ratio, hysteresis)
- **Proof of Concept:** Individual CNTFETs were already used to derive a stable PUF response
- **Susceptibility to Defects:** A leaky/fault CNTFET perturbs the entire structure
- **Read-out Complexity:** Requires high-precision equipment to measure current

Methodology and Progress

Measurements

- **Transfer Characteristics:** Experimentally determine relationship between drain current I_D and voltages V_{DS} and V_{GS}
- **On-wafer probing:** Using probing station and 28-needle probe-card
- Characterized more than 100 different crossbar arrays
- **Challenge confirmed:** Measured currents in array are washier than individually probed CNTFETs
- Single threshold quantization yields acceptable, but not perfect uniformity



Future Steps

Plan of Research

Leakage Localization

- Development of equivalent circuit model through measurement data
- Feedback for fabrication and selection of representative CNTFETs

Voltage-Readout Active Switch Matrix

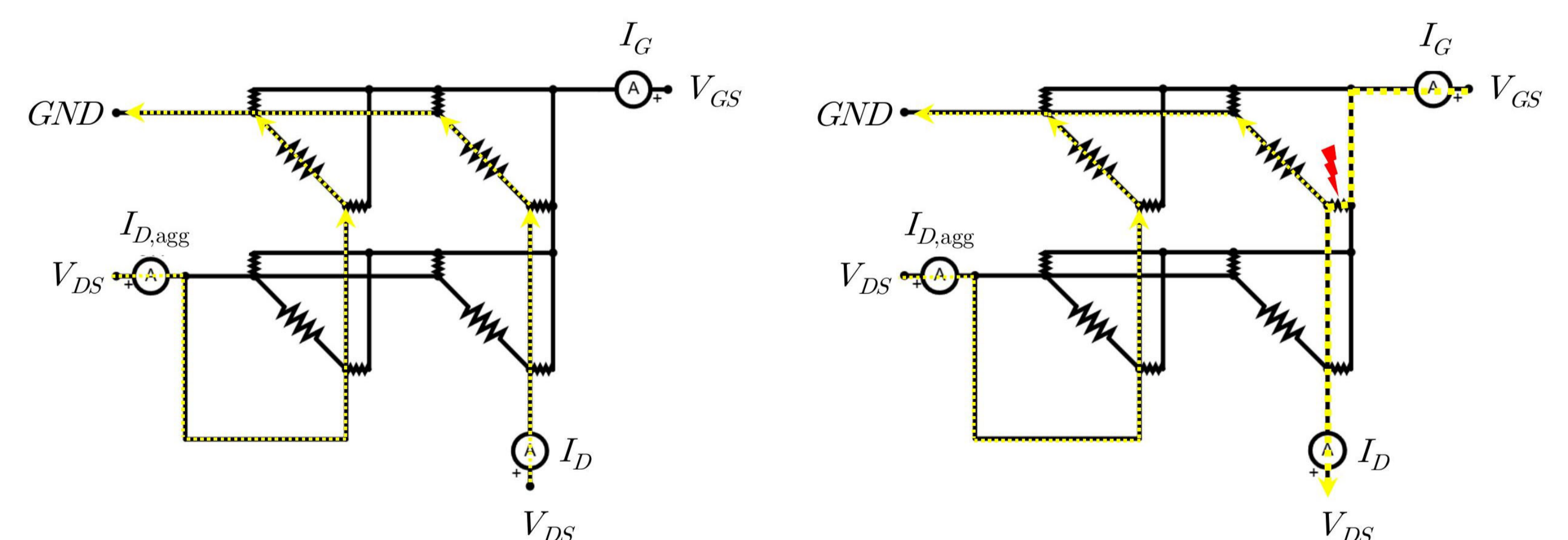
- **Selective Activation:** Pairing of CNTFETs with thin-film FETs gating its source and gate terminals
- **Voltage-Readout:** Drain voltage used for ternary PUF quantization

FPGA Interfacing

- **Analog-to-Digital Conversion:** Output voltage is input to FPGA (e.g. Xilinx Zynq UltraScale+ RFSoc series) to perform PUF quantization
- **Key Extraction:** Post-processing performed in FPGA

Security Evaluation

- **Electromagnetic analysis and injection:** Targeting serial and parallel read-out logic on FPGA
- **Optical Probing:** Photon emission microscopy to detect switching activity during read-out
- **PUF quality:** Spatial correlation of responses within crossbar array



Previous Relevant Works

- [1] S. Böttger, F. Frank *et al.*, CNT-PUFs: Highly Robust and Heat-Tolerant Carbon-Nanotube-Based Physical Unclonable Functions, in: 2023 IEEE NANO Conference.
- [2] N. Mexis *et al.*, Spatial Correlation in Weak Physical Unclonable Functions: A Comprehensive Overview, in: 2023 DSD Conference.

Acknowledgements

This work is partially supported by the German Research Foundation (DFG) within the priority program „Nano Security: From Nano-Electronics to Secure Systems“ (SPP 2253) under project „NANOSEC²: Nanomaterial-based platform electronics for PUF circuits with extended entropy sources“ (439892735).