HW-SW management using a lightweight Yocto-based OS on a ZCU102

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[2] Abinsula S.R.L.

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Introduction – Motivation

Introduction – Motivation

Flexibility	Performance
Programmability	Energy efficiency

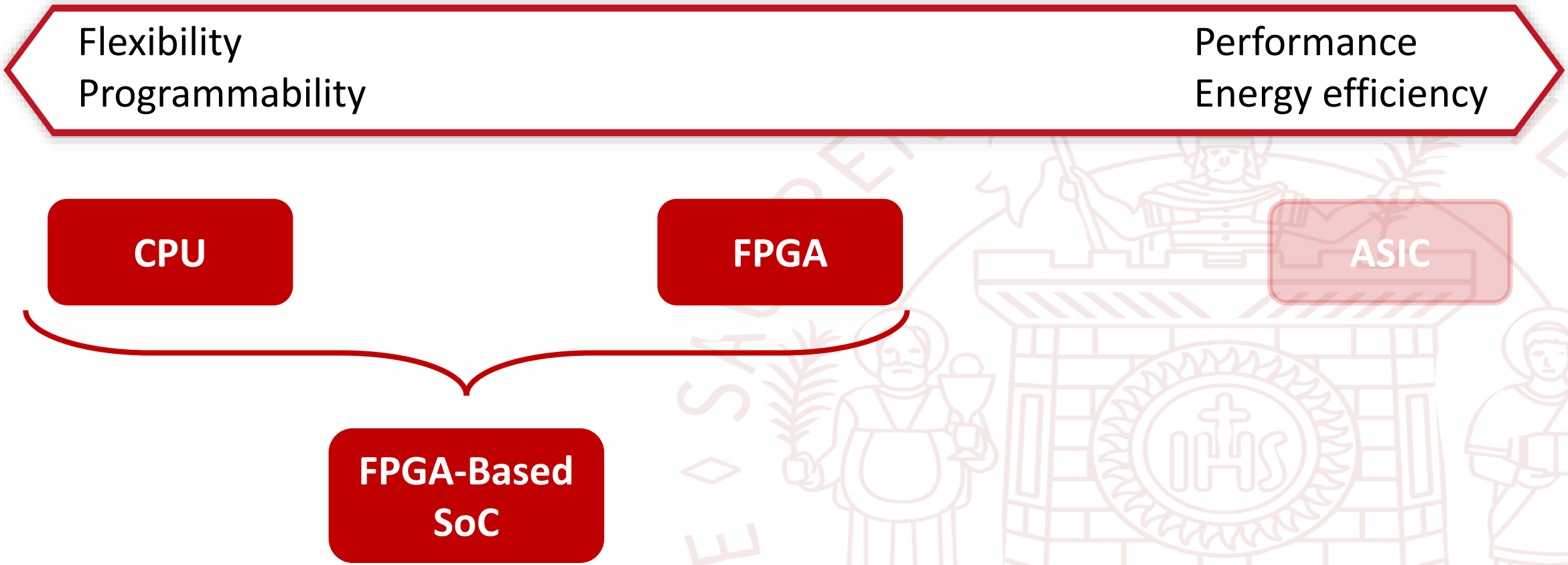
Introduction – Motivation

Flexibility
Programmability

Performance
Energy efficiency

CPU **FPGA** **ASIC**

Introduction – Motivation



Introduction – Motivation

How to make them collaborate?

Introduction – Proposed methodology

Introduction – Proposed methodology

Customizable OS

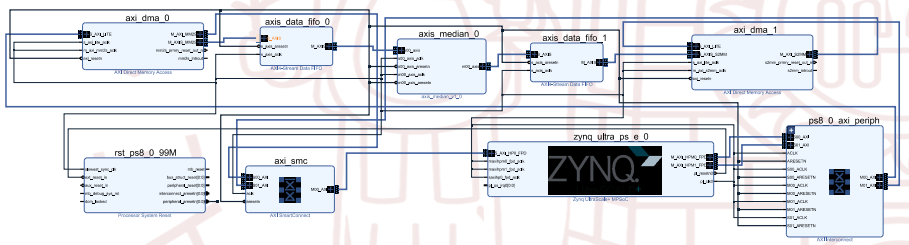
yocto PROJECT

Introduction – Proposed methodology

Customizable OS → **HW accelerator design**

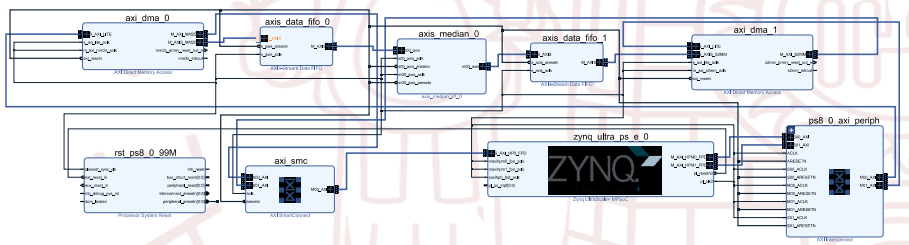
Introduction – Proposed methodology

Customizable OS → **HW accelerator design** → **HW-SW system design**



Introduction – Proposed methodology

Customizable OS → **HW accelerator design** → **HW-SW system design** → **Testing architecture**



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Proposed methodology – Customizable OS

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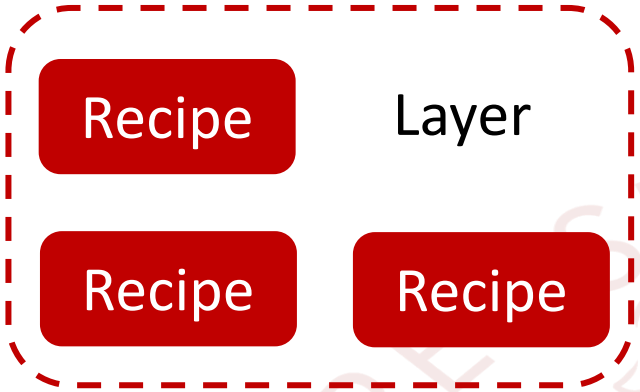
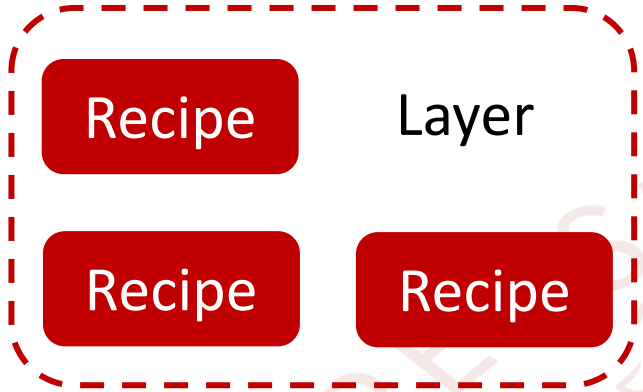
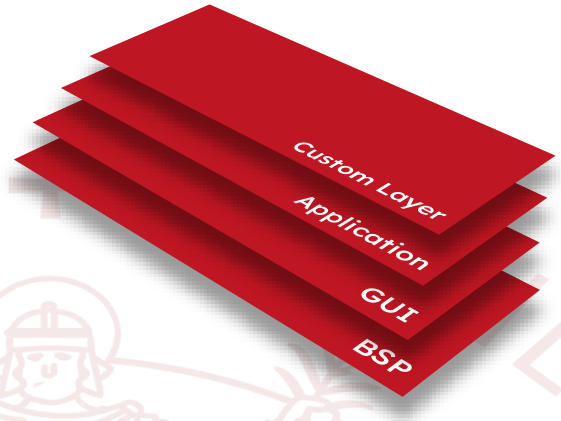


Proposed methodology – Customizable OS

yocto PROJECT





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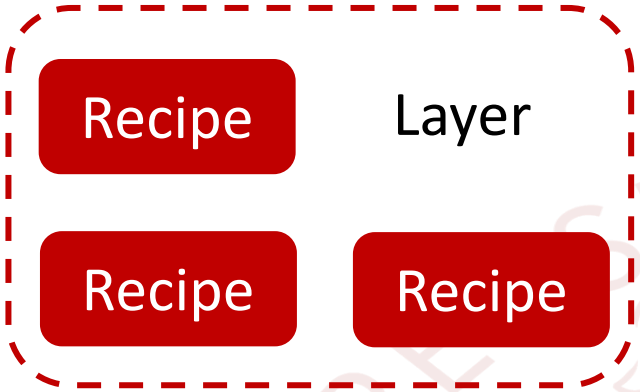

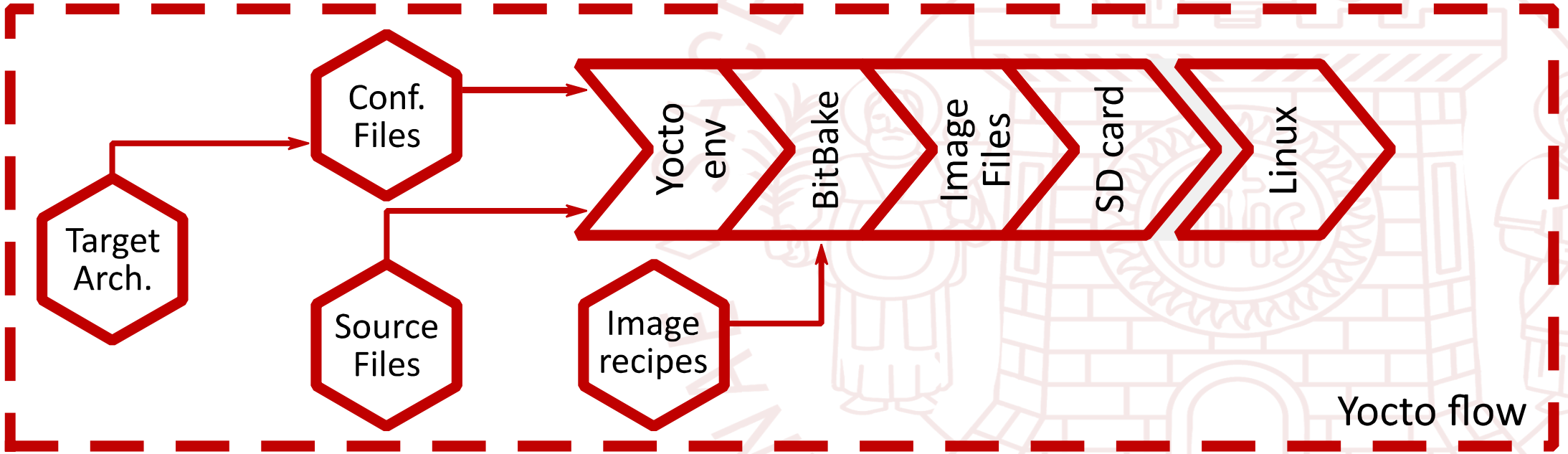

Proposed methodology – HW accelerator design

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Multi-Dataflow Composer

UNISS + UNICA

https://github.com/mdc-suite

Proposed methodology – HW accelerator design

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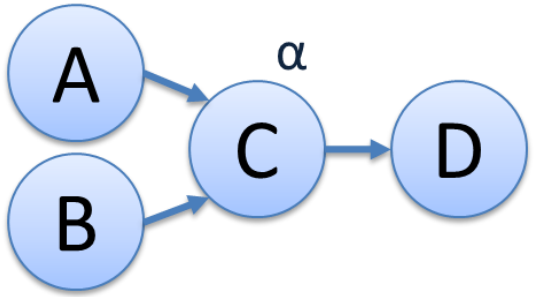

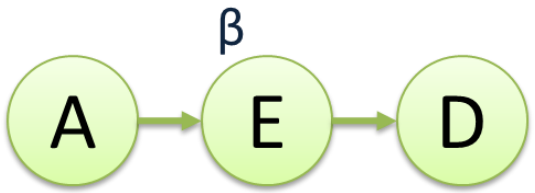

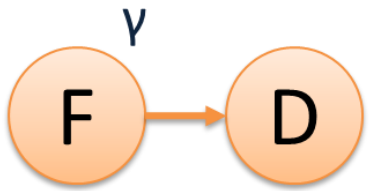

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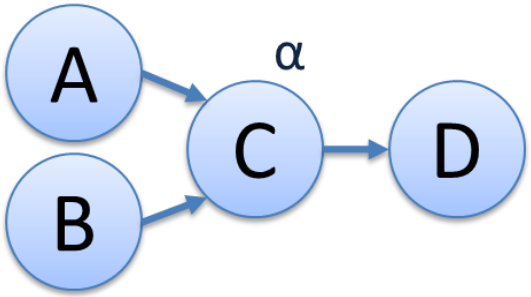

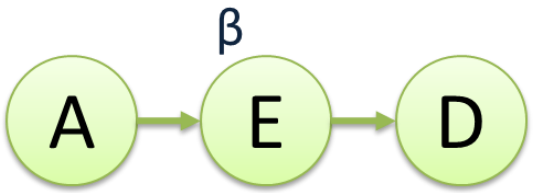

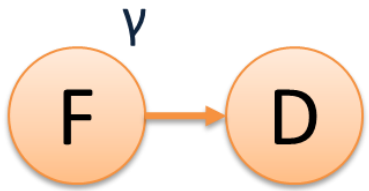

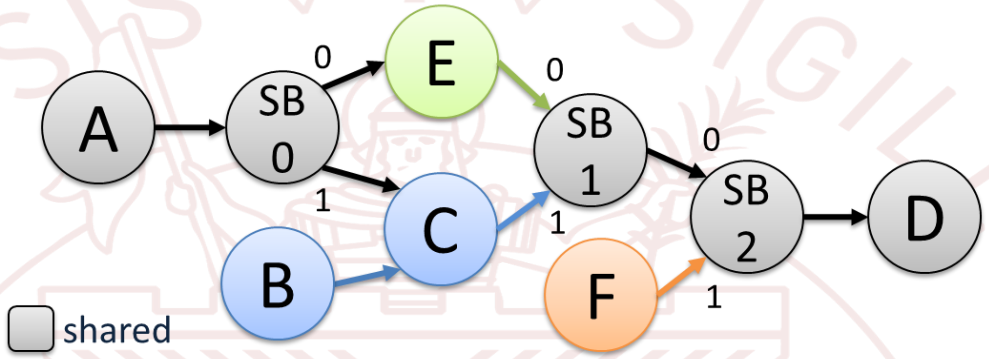

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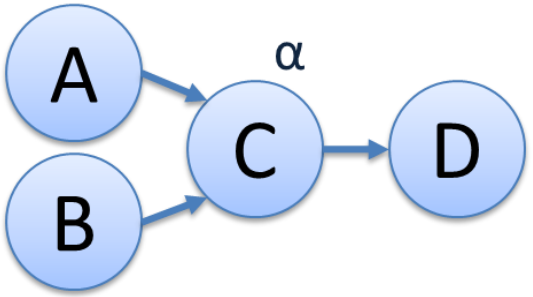

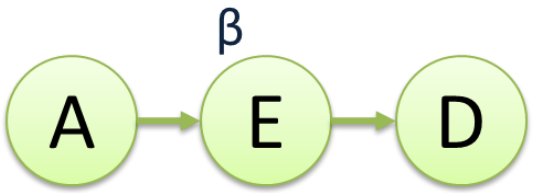

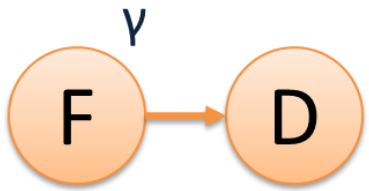

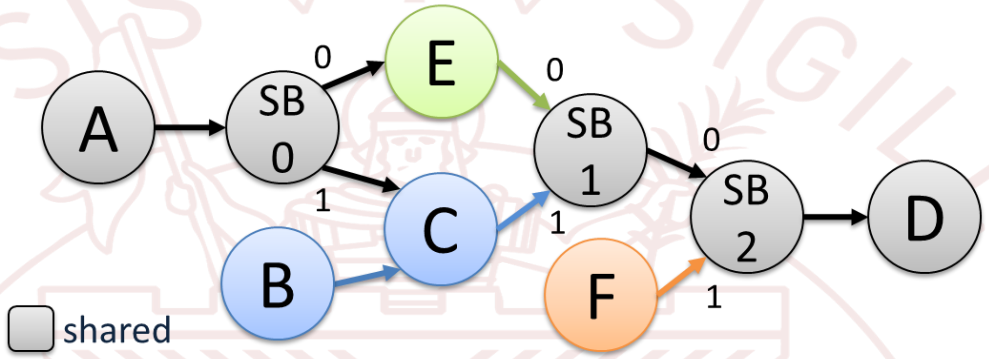

SB	0	1	2
α	1	1	0
β	0	0	0
γ	x	x	1

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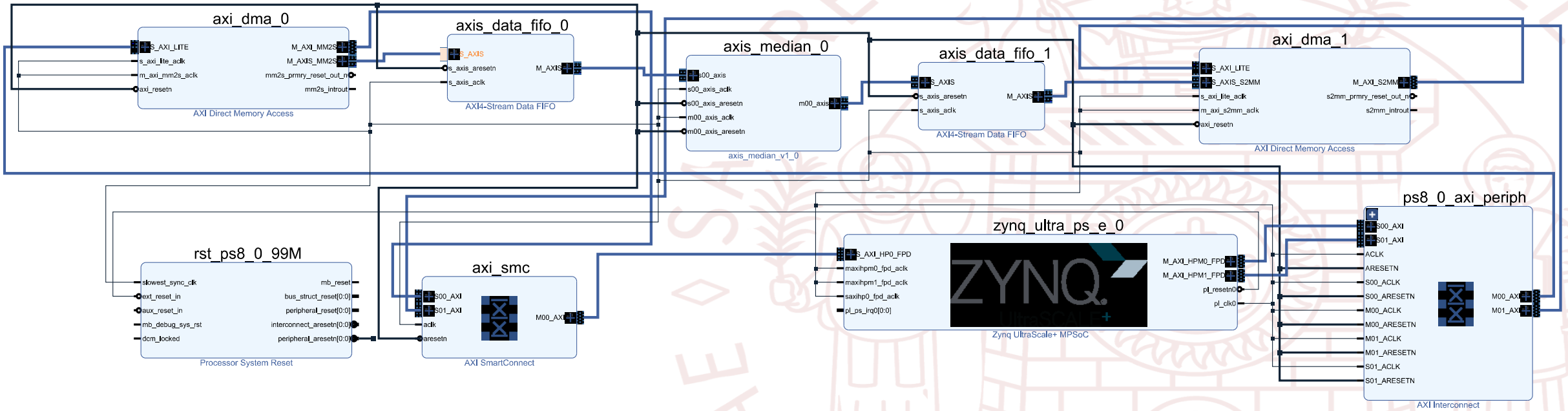
Proposed methodology – HW accelerator design

Multi-Dataflow Composer



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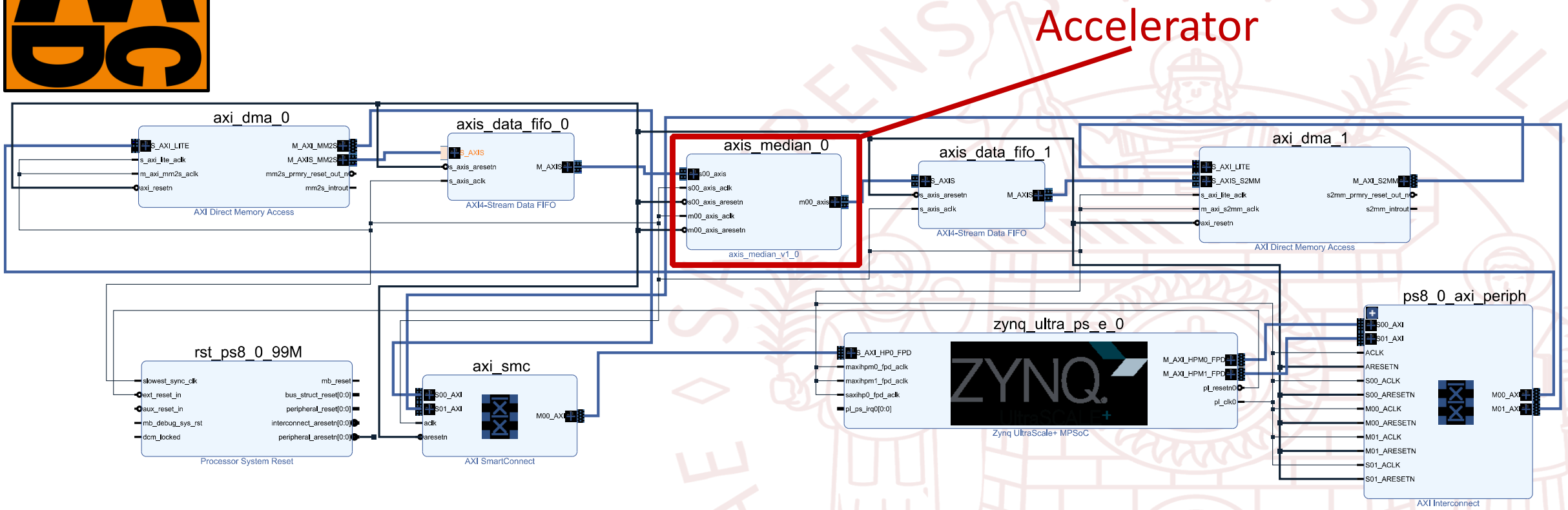

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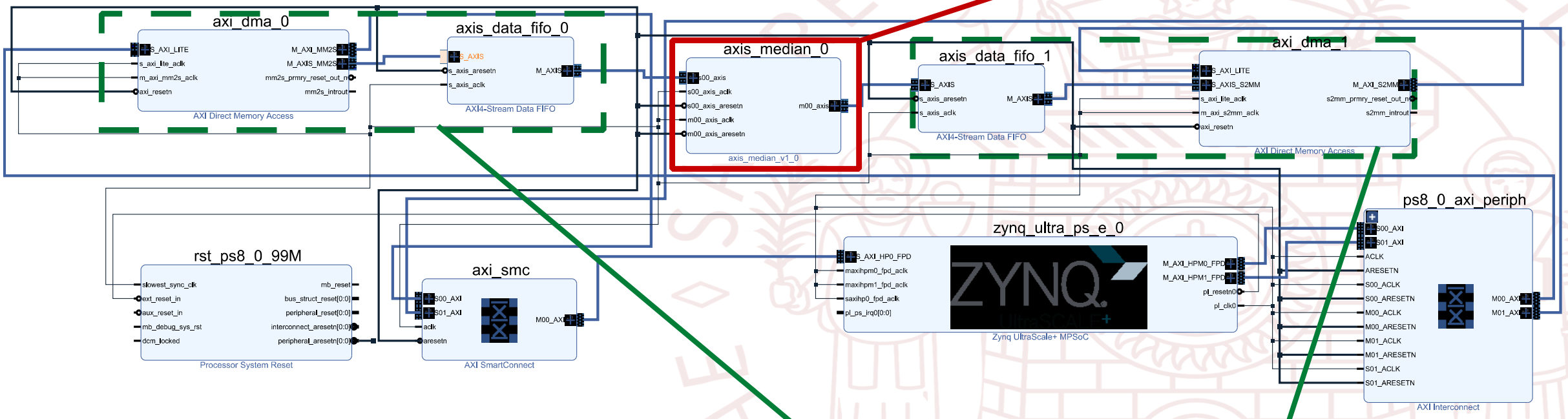

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Proposed methodology – HW accelerator design

Multi-Dataflow Composer

- ✓ Dataflow-based design
- ✓ Multi-Dataflow accelerator

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Proposed methodology – HW accelerator design

Multi-Dataflow Composer

- ✓ Dataflow-based design
- ✓ Multi-Dataflow accelerator
- ✓ Co-Processor infrastructure
- ✓ Vivado scripts

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Proposed methodology – HW accelerator design

Multi-Dataflow Composer

- ✓ Dataflow-based design
- ✓ Multi-Dataflow accelerator
- ✓ Co-Processor infrastructure
- ✓ Vivado scripts
- ✓ SW APIs

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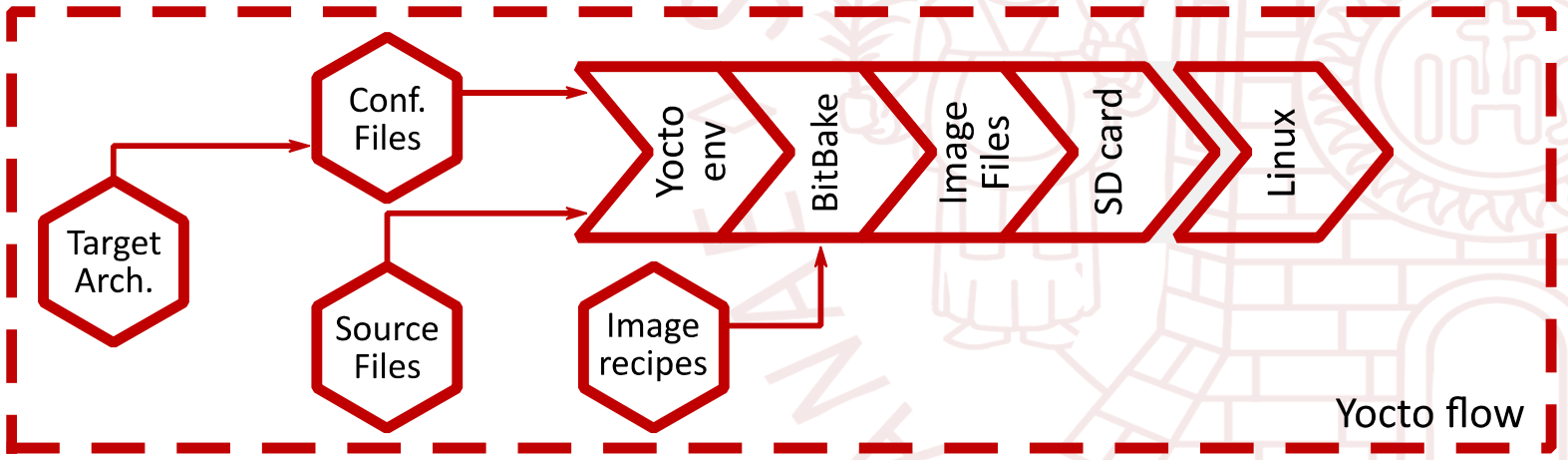
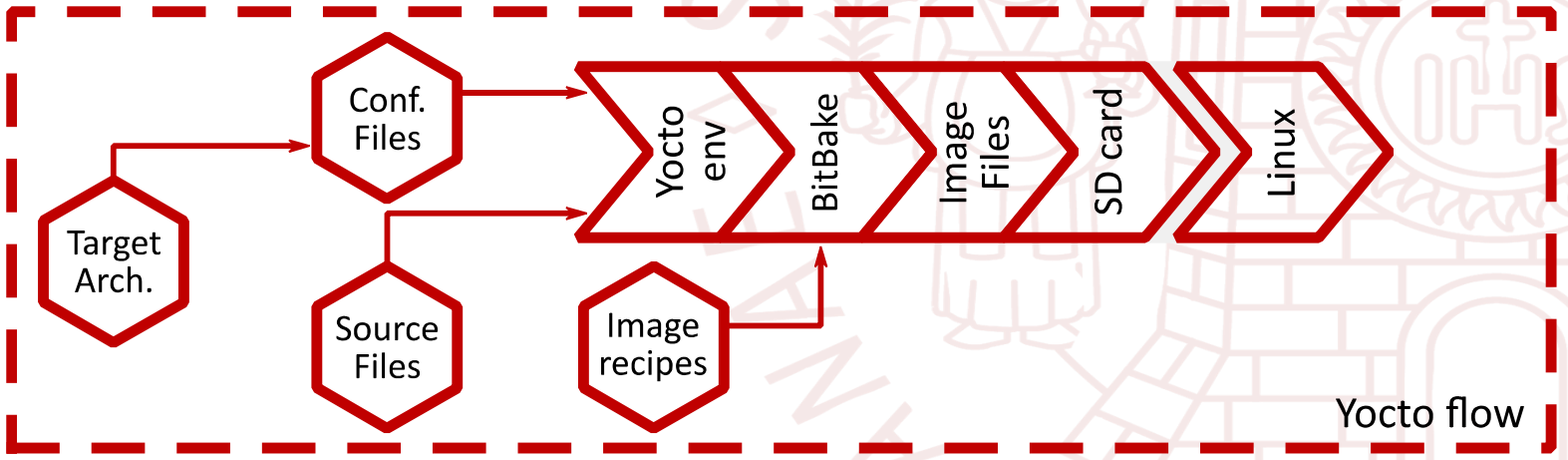
Proposed methodology



Proposed methodology

- **Yocto flow:**
  - Select the target architecture
  - Select the layers to be included
  - Bitbake



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- **Yocto flow:**
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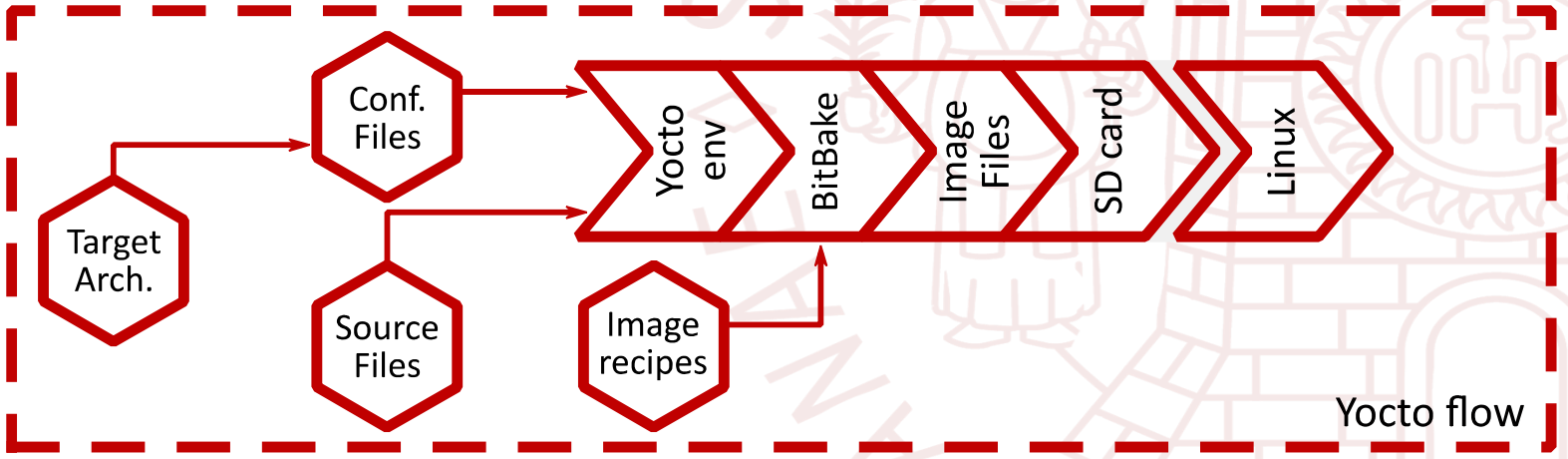
- **Create the HW accelerator with MDC**



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- **Yocto flow:**
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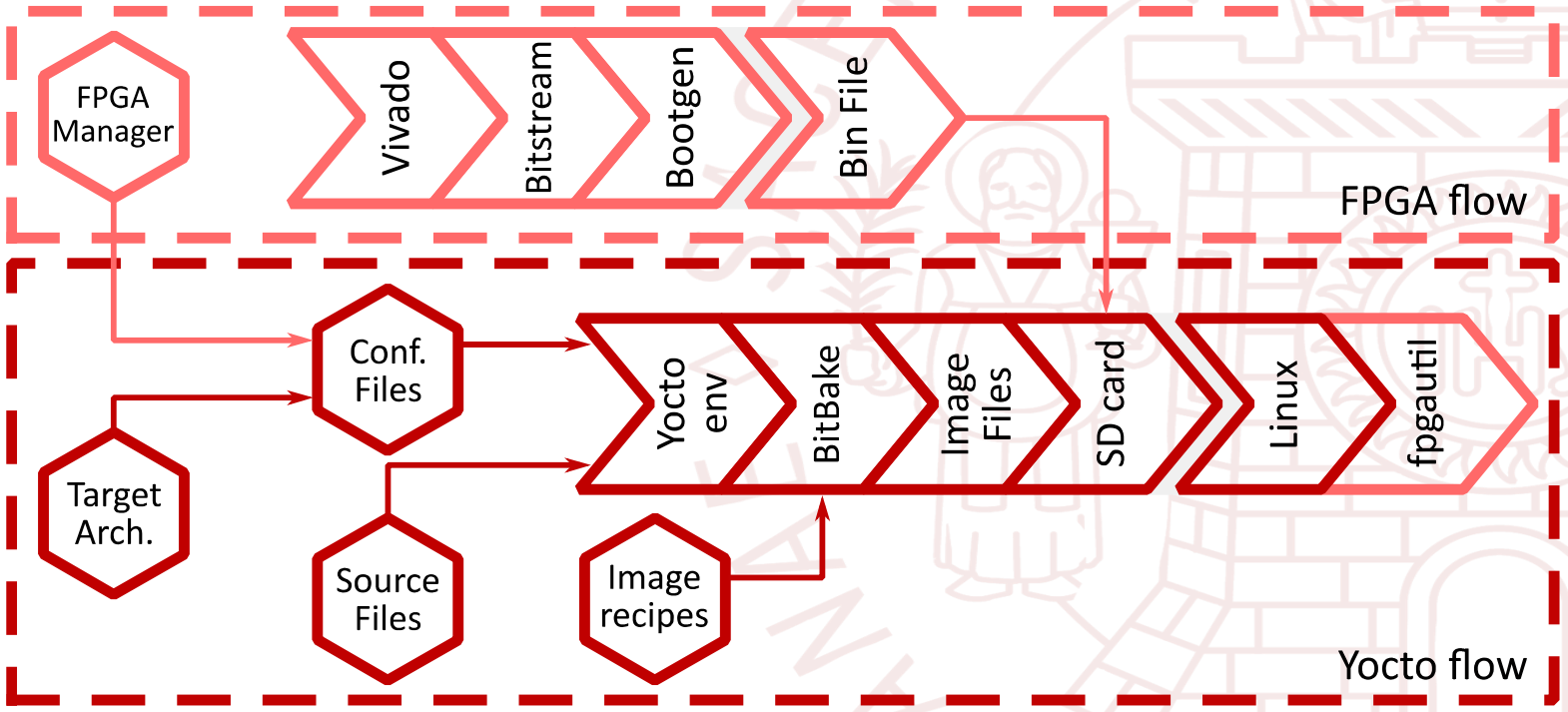
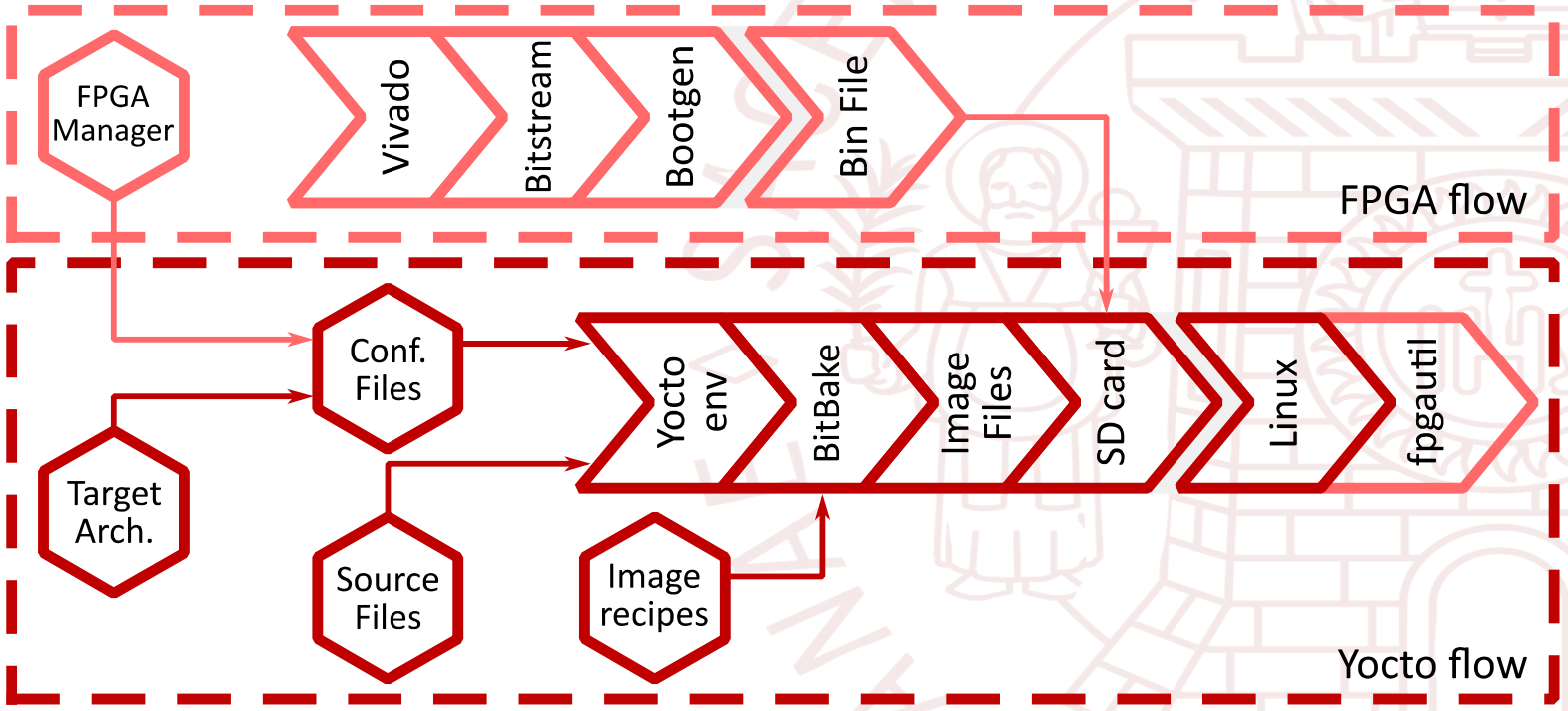
- **FPGA flow:**
  - Include the accelerator in Vivado
  - Generate the bitstream and the binary file



Proposed methodology

- **Yocto flow:**
  - Select the target architecture
  - Select the layers to be included
  - Bitbake
- **Create the HW accelerator with MDC**
- **FPGA flow:**
  - Include the accelerator in Vivado
  - Generate the bitstream and the binary file
- **Yocto flow:**
  - Burn the SD card
  - Use it



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Assessment – Context

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- Comp4Drones ECSEL JU Project: Precision Agriculture
  - FPGA-Based on-board real-time processing
  - ZCU102 FPGA

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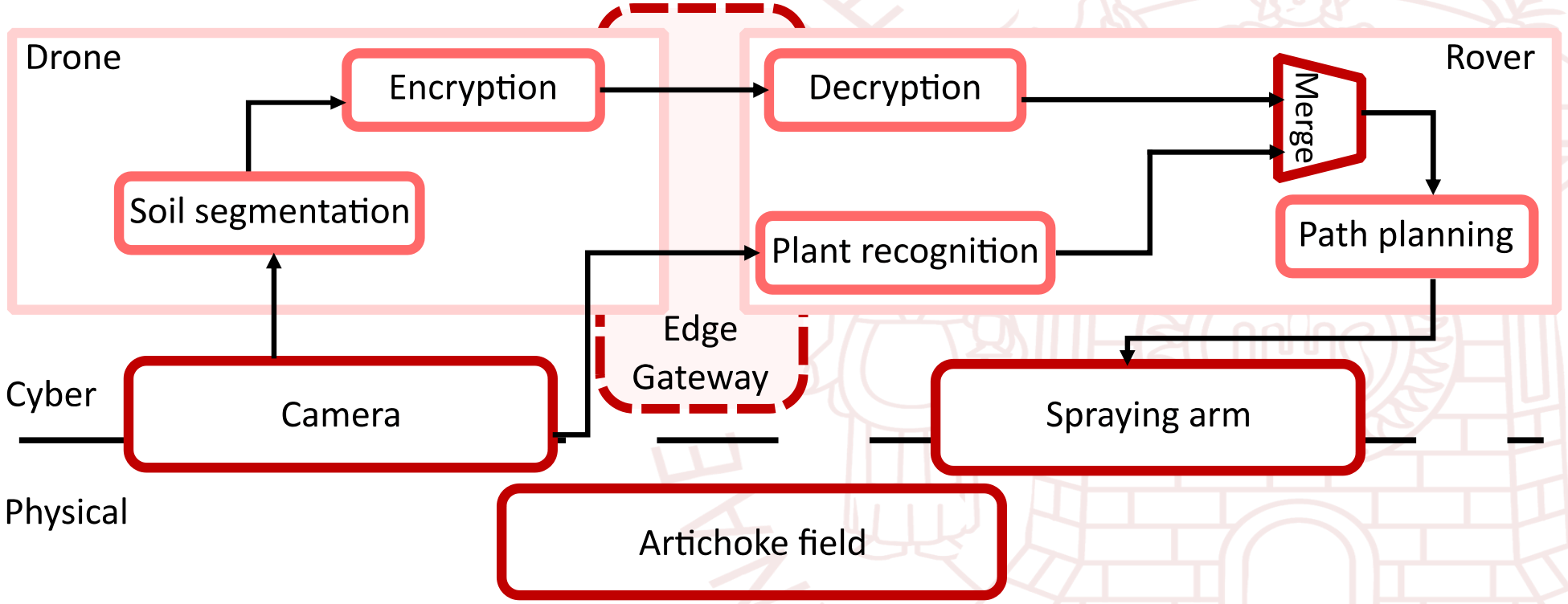
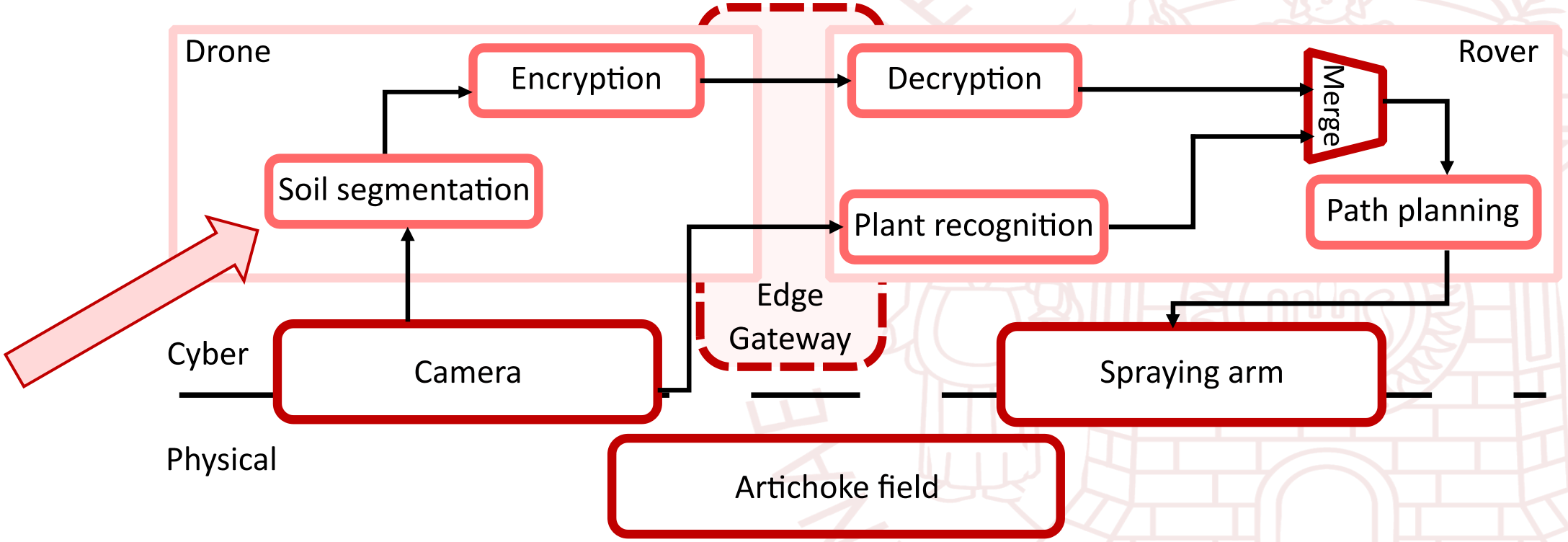


Assessment – Context

- Comp4Drones ECSEL JU Project: Precision Agriculture
  - FPGA-Based on-board real-time processing
  - ZCU102 FPGA
  - Soil Segmentation

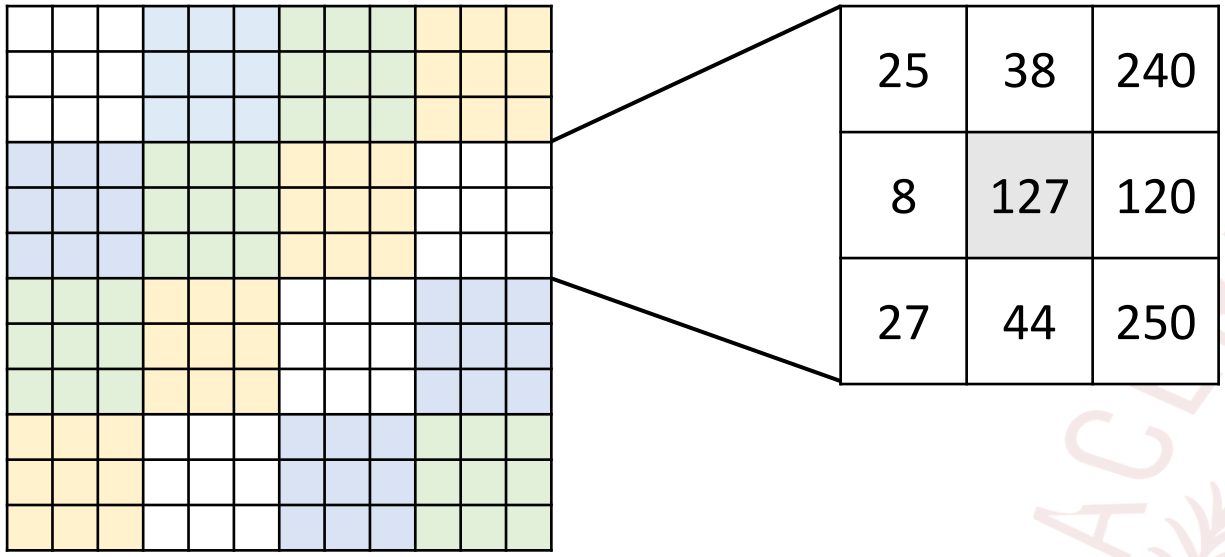


Assessment – Algorithm

Median filter – Box-based filtering

Assessment – Algorithm

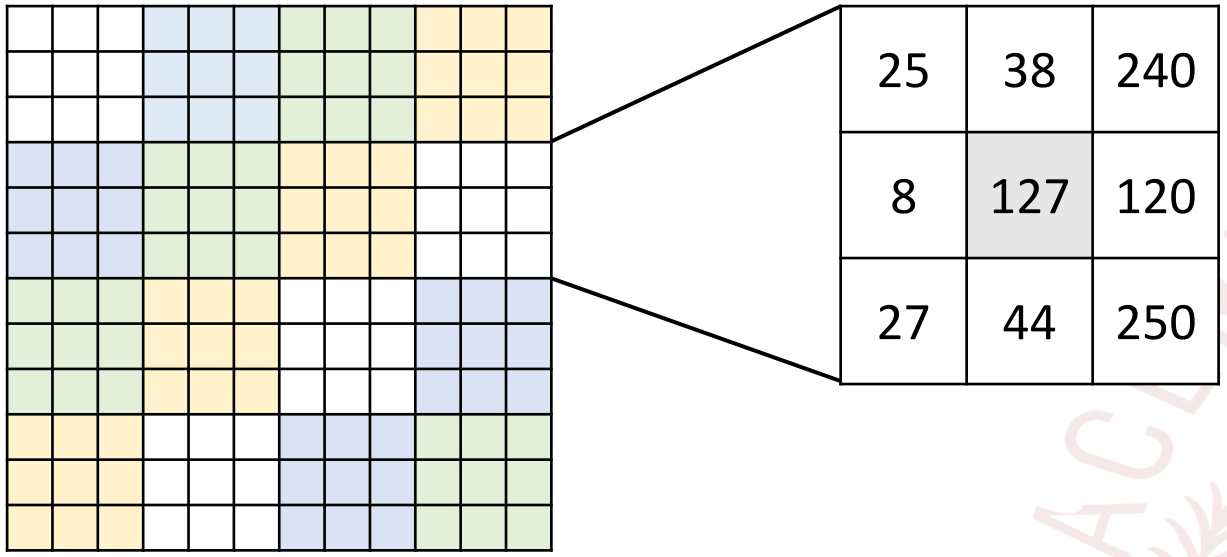
Median filter – Box-based filtering



25	38	240
8	127	120
27	44	250

Assessment – Algorithm

Median filter – Box-based filtering



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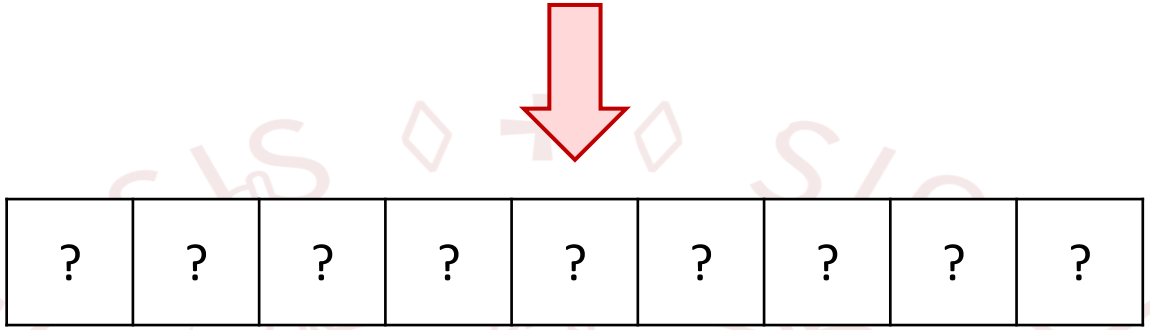

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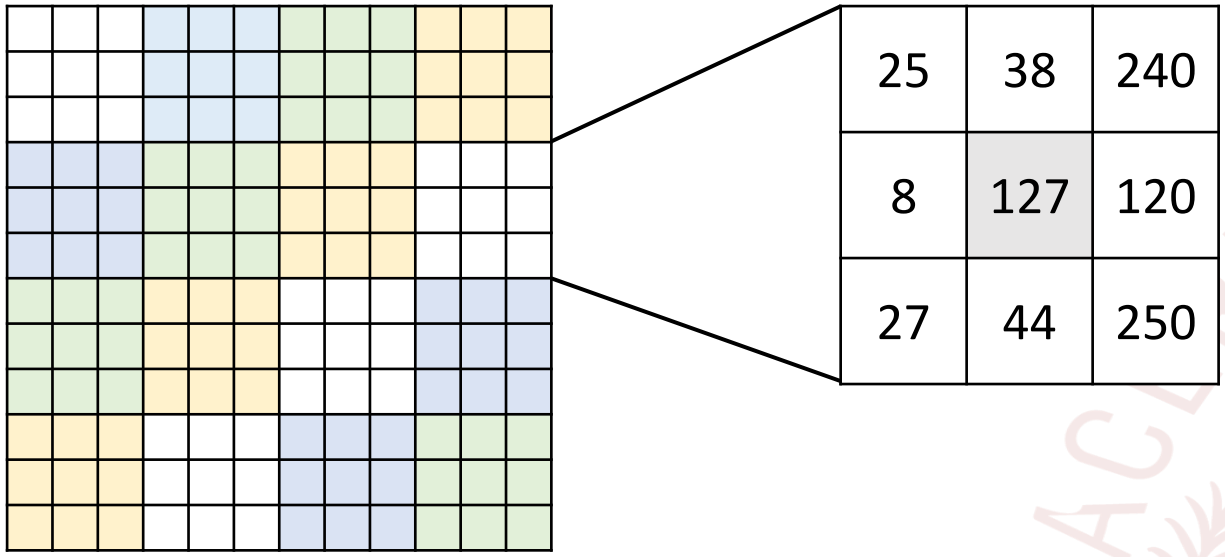

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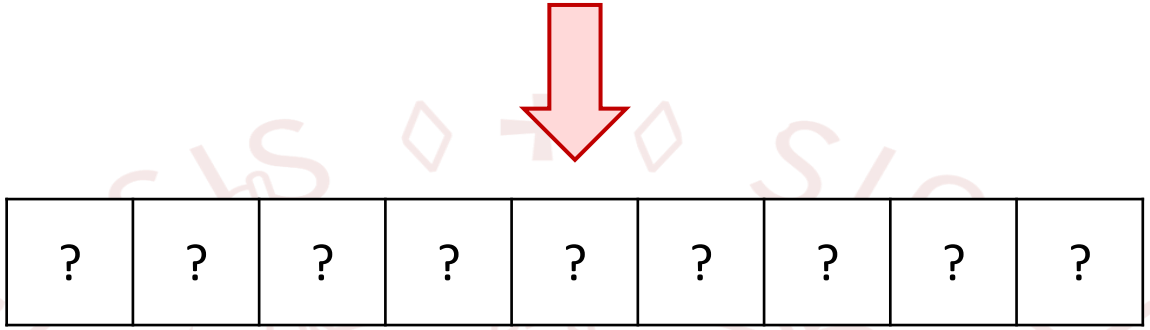


Round 1

Pivot: 128

Larger:

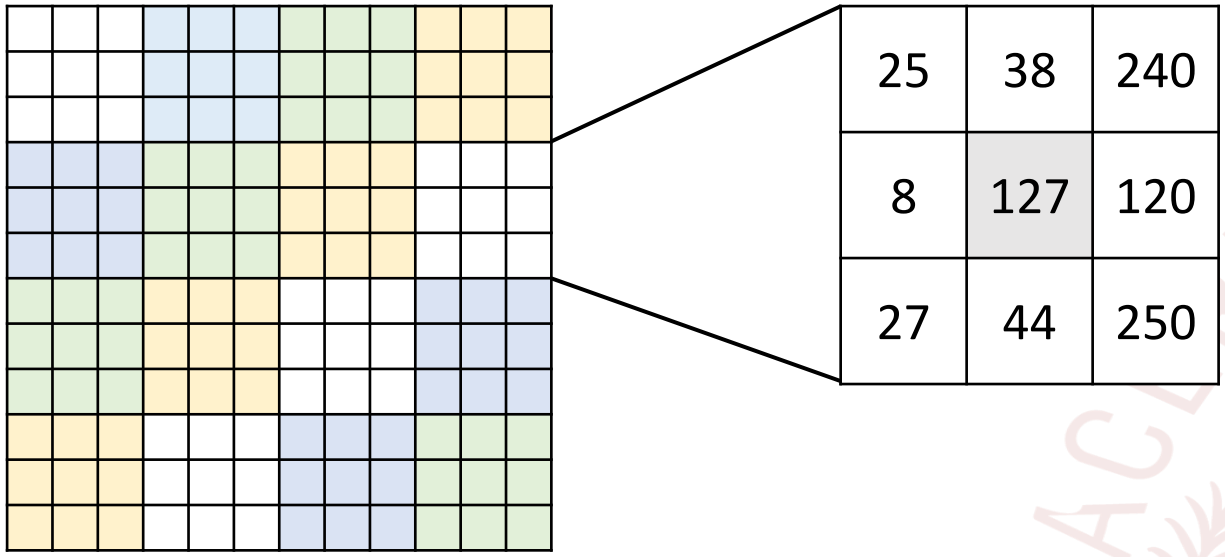
240	250

Lower:

25	38	8	127	120	27	44

Assessment – Algorithm

Median filter – Box-based filtering



25	38	240
8	127	120
27	44	250

?	?	?	?	?	?	?	?	?

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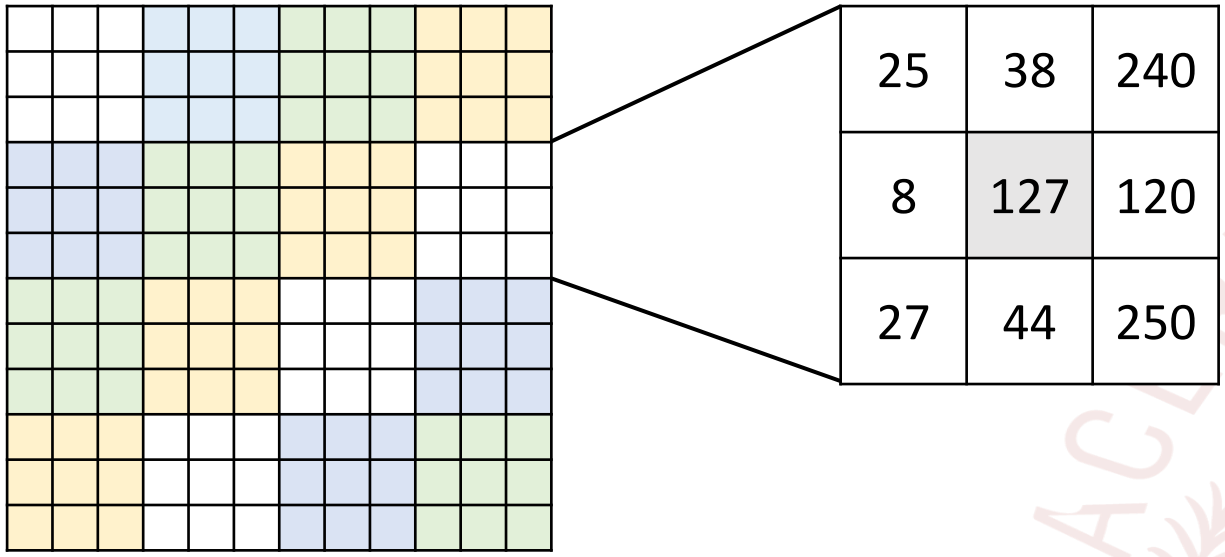


25	38	240
8	127	120
27	44	250

?	?	?	?	?	?	?	?	?

Round 1

Pivot: 128

Larger:

240	250

Lower:

25	38	8	127	120	27	44

Round 2

Pivot: (127+8)/2 = 62

Larger:

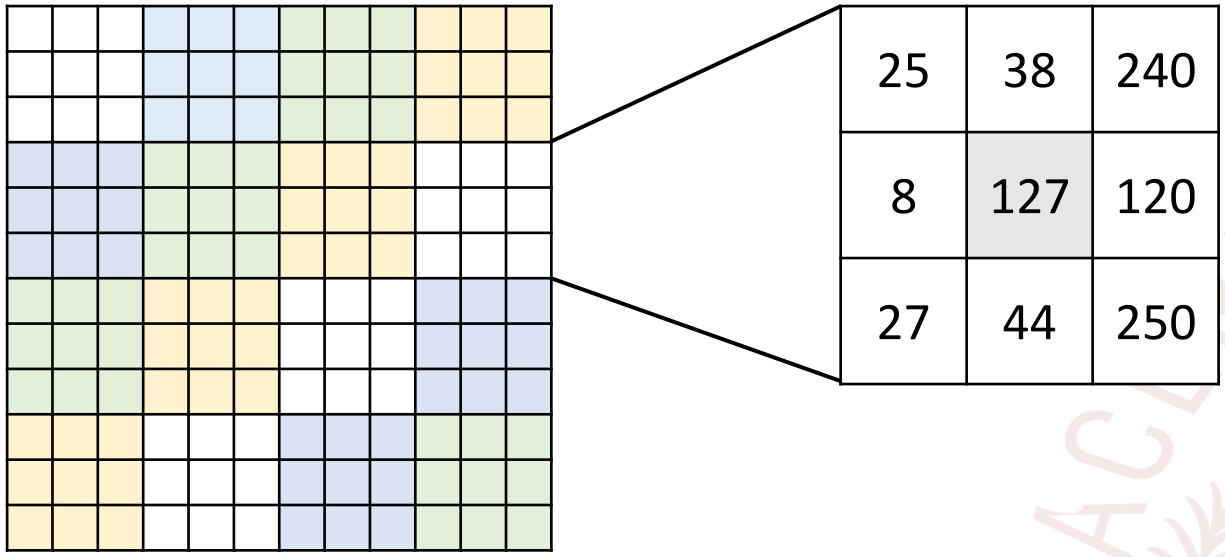
127	120

Lower:

25	38	8	27	44

Assessment – Algorithm

Median filter – Box-based filtering



25	38	240
8	127	120
27	44	250

?	?	?	?	44	?	?	?	?

Round 1

Pivot: 128

Larger:

240	250

Lower:

25	38	8	127	120	27	44

Round 2

Pivot: (127+8)/2 = 62

Larger:

127	120

Lower:

25	38	8	27	44

Round 3
Median = 44

Assessment – Results

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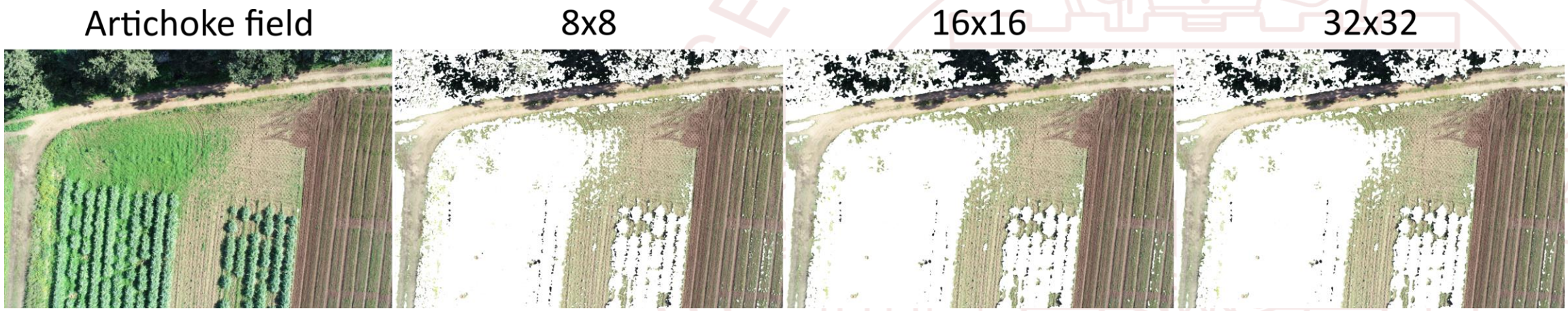
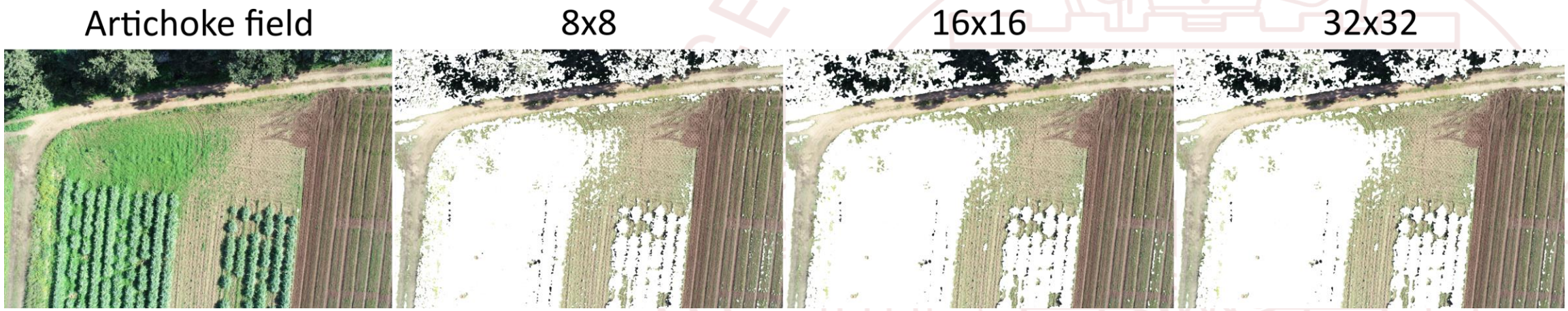
- Comp4Drones ECSEL JU Project: Precision Agriculture
  - Artichoke field – Soil Segmentation



Assessment – Results

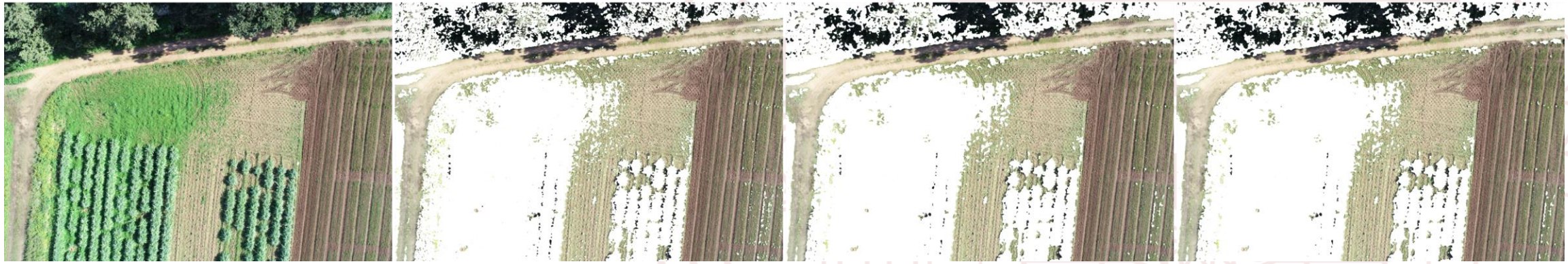
- Comp4Drones ECSEL JU Project: Precision Agriculture
  - Artichoke field – Soil Segmentation
  - Speedup up to 1.55× (HW vs SW) with different box sizes



Assessment – Results

- Comp4Drones ECSEL JU Project: Precision Agriculture
  - Artichoke field – Soil Segmentation
  - Speedup up to 1.55× (HW vs SW) with different box sizes
  - Same accuracy (HW vs SW)

Artichoke field | 8x8 | 16x16 | 32x32



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Conclusions and future work

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- ✓ MDC: ease HW accelerator design
- ✓ MDC: generate HW-SW system and SW APIs
- ✓ YOCTO: customizable OS
- ✓ System validated in precision agriculture (Comp4Drones)
- ✓ Acceleration of 1.55×

Conclusions and future work

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- ➢ Precision agriculture: implement the whole Comp4Drones Use-Case
- ➢ OS connection with drone autopilot

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- ✓ Acceleration of 1.55×

- ➢ Precision agriculture: implement the whole Comp4Drones Use-Case
- ➢ OS connection with drone autopilot

- ➢ Testing in other fields (e.g. Automotive)
- ➢ Multithreading support

Questions?

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