CEI UPM | Centro de Electrónica Industrial

Fine Grain Reconfiguration: the ARTICo³ Framework

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POLITÉCNICA

ARTICo³: Motivation

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Tasks

Independent of the task itself!

Put as many people as possible to work, and save time

Replicate xN
Multithreaded solutions
HPC-like approach

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Do not tell others what you are doing, protect from others

Duplicate
Dual-rail techniques for side-channel attack protection

ARTICo^3: Motivation

Tasks  + Requirement

Independent of the task itself!

Urgent	Confidential	Critical
Put as many people as possible to work, and save time	Do not tell others what you are doing, protect from others	Let more than one do the same work and compare result
Replicate xN Multithreaded solutions HPC-like approach	**Duplicate** Dual-rail techniques for side-channel attack protection	**Replicate x2 or x3** (+ voter unit) DMR and TMR

ARTICo³: Motivation

Tasks

Requirement

Independent of the task itself!

Urgent

Put as many people as possible to work, and save time

Confidential

Do not tell others what you are doing, protect from others

Critical

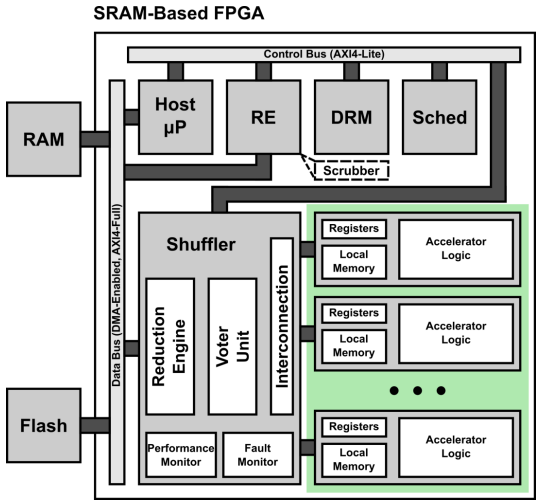
Let more than one do the same work and compare result

Dynamic and Partial Reconfiguration (hardware acceleration + module replication)

What is required?

High Performance Embedded Computing Platforms

Architectures

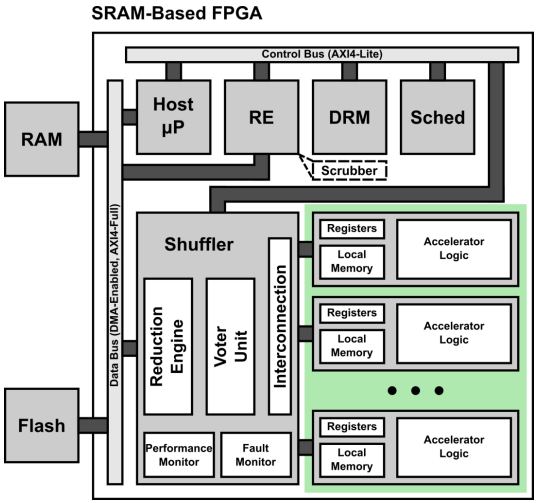


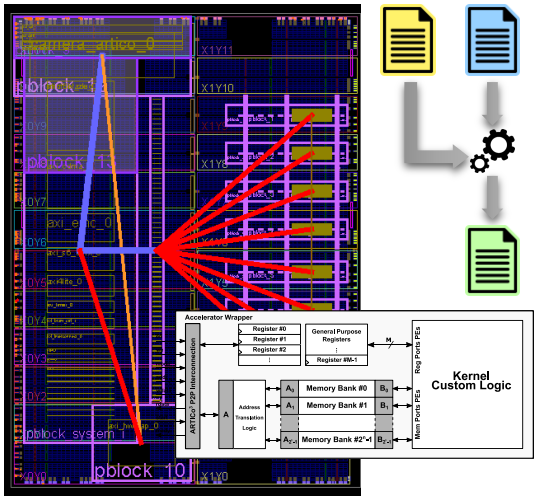
What is required?

High Performance Embedded Computing Platforms

Architectures

Design Flows

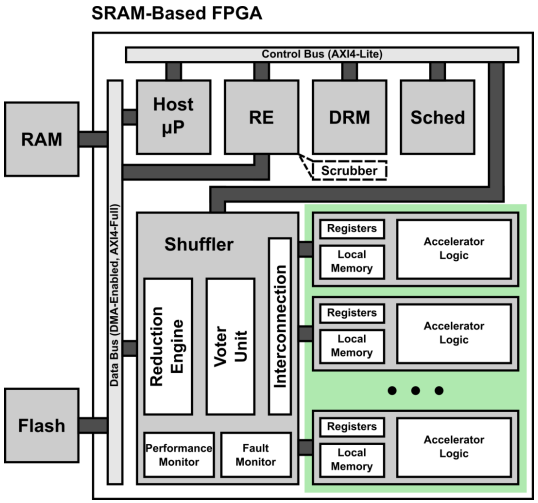




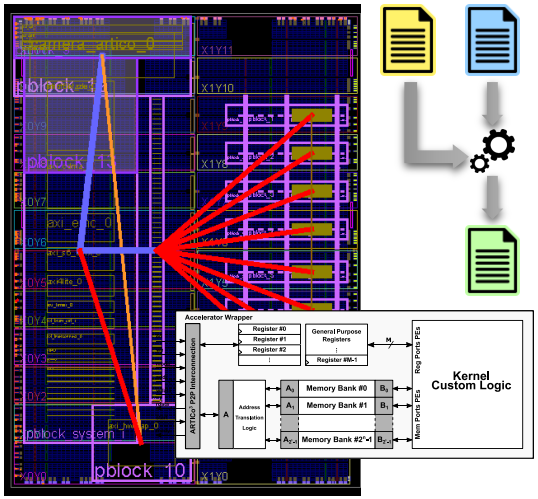
What is required?

High Performance Embedded Computing Platforms

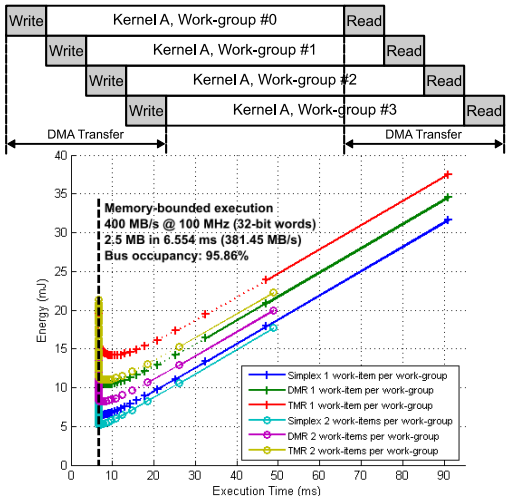
Architectures



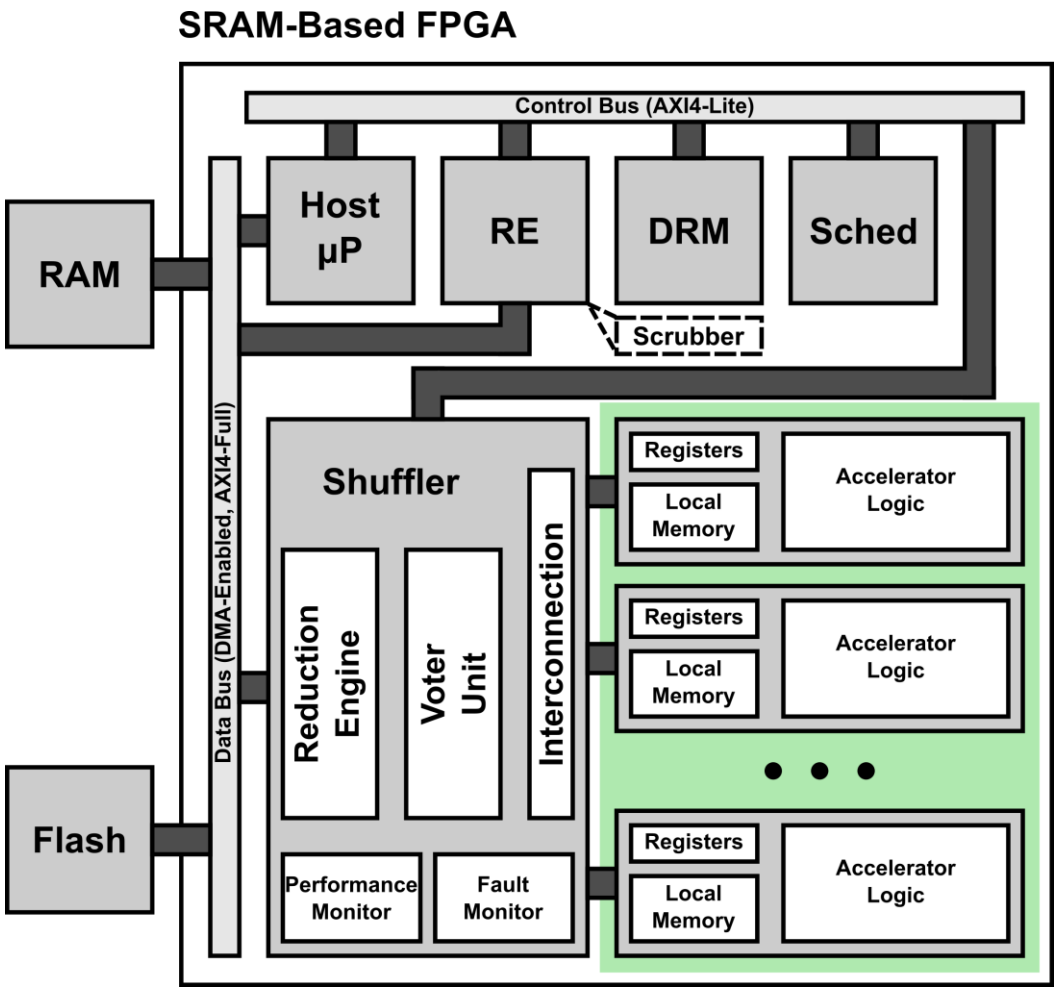
Design Flows



Runtime Environment

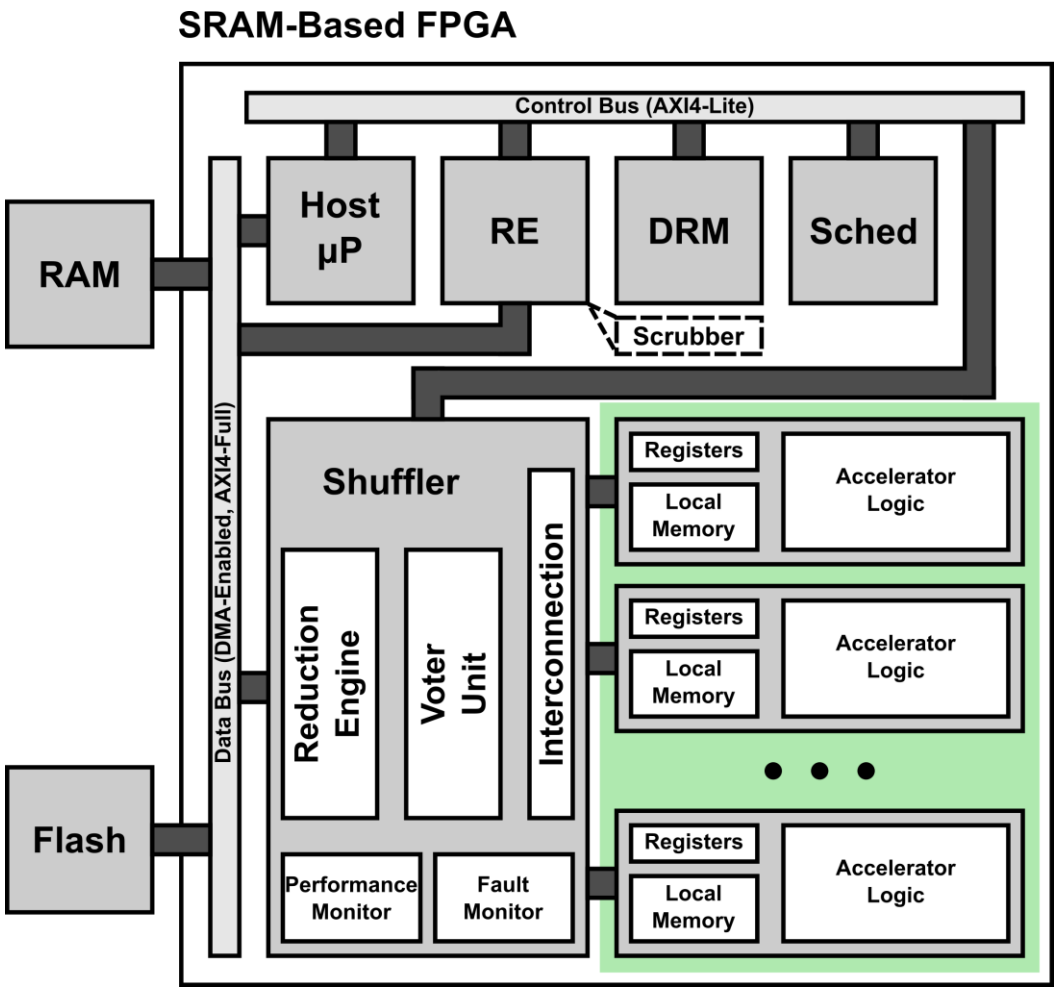


ARTICo^3 Architecture



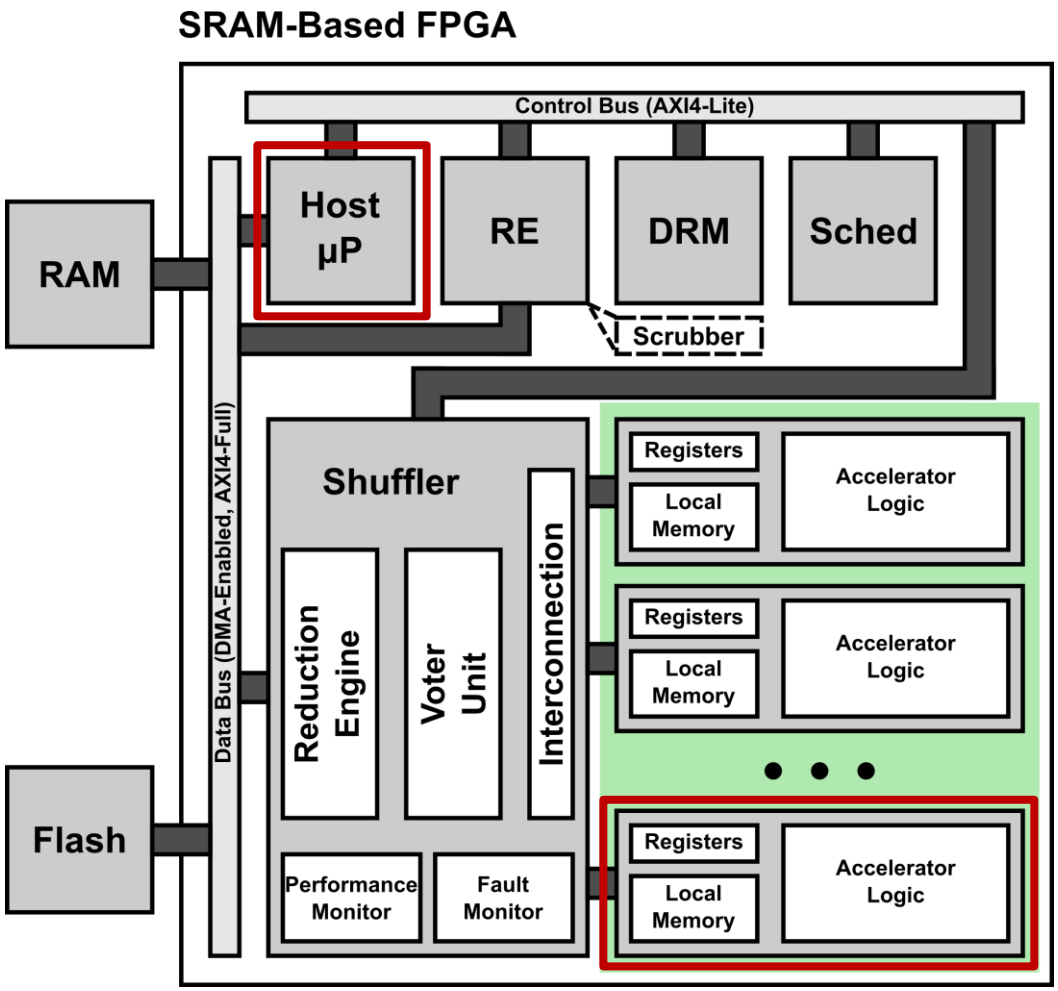
Arquitectura
Reconfigurable para el
Tratamiento
Inteligente de
Cómputo
Consumo
Confiabilidad

ARTICo³ Architecture



Reconfigurable
Architecture to enable
Smart
Management of
Performance
Energy Consumption
Dependability

ARTICo³ Architecture



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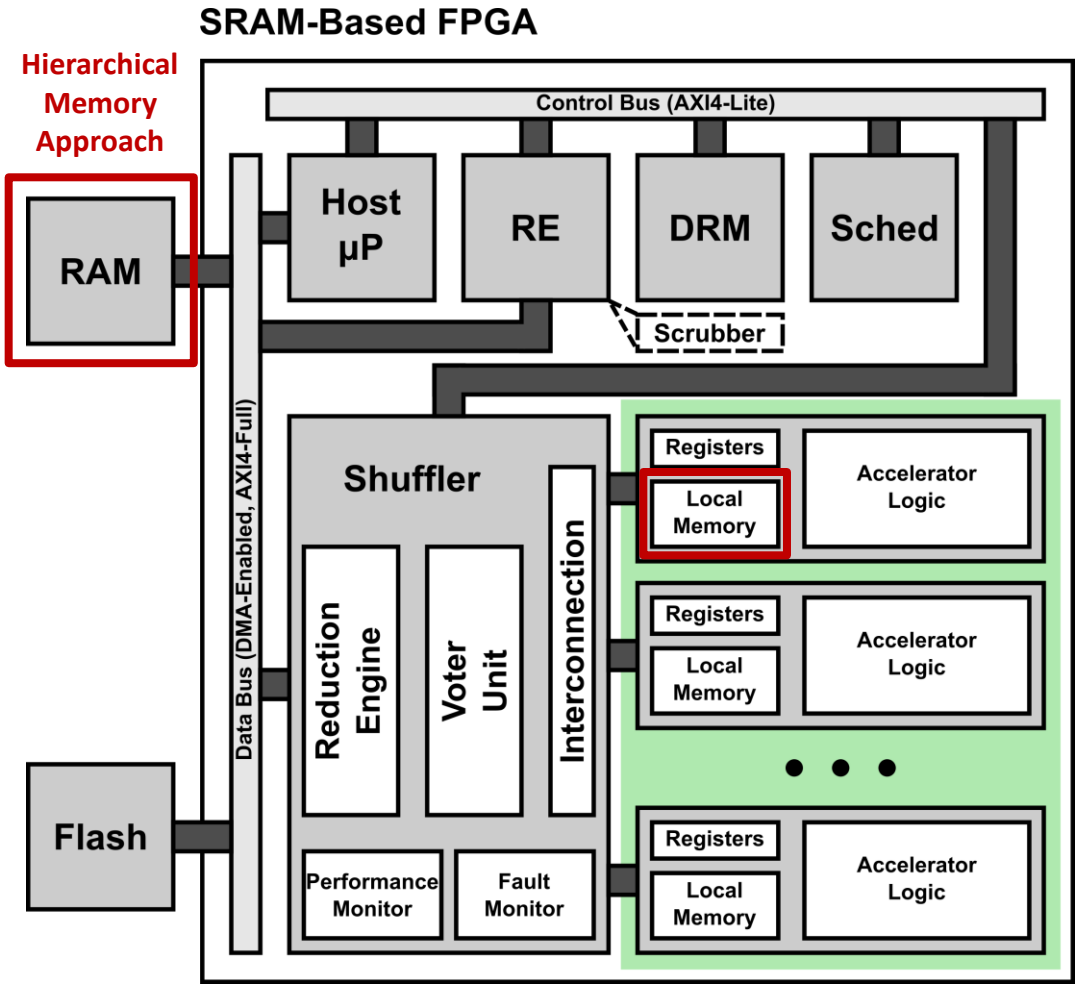
Hardware Acceleration

ARTICo³ Architecture



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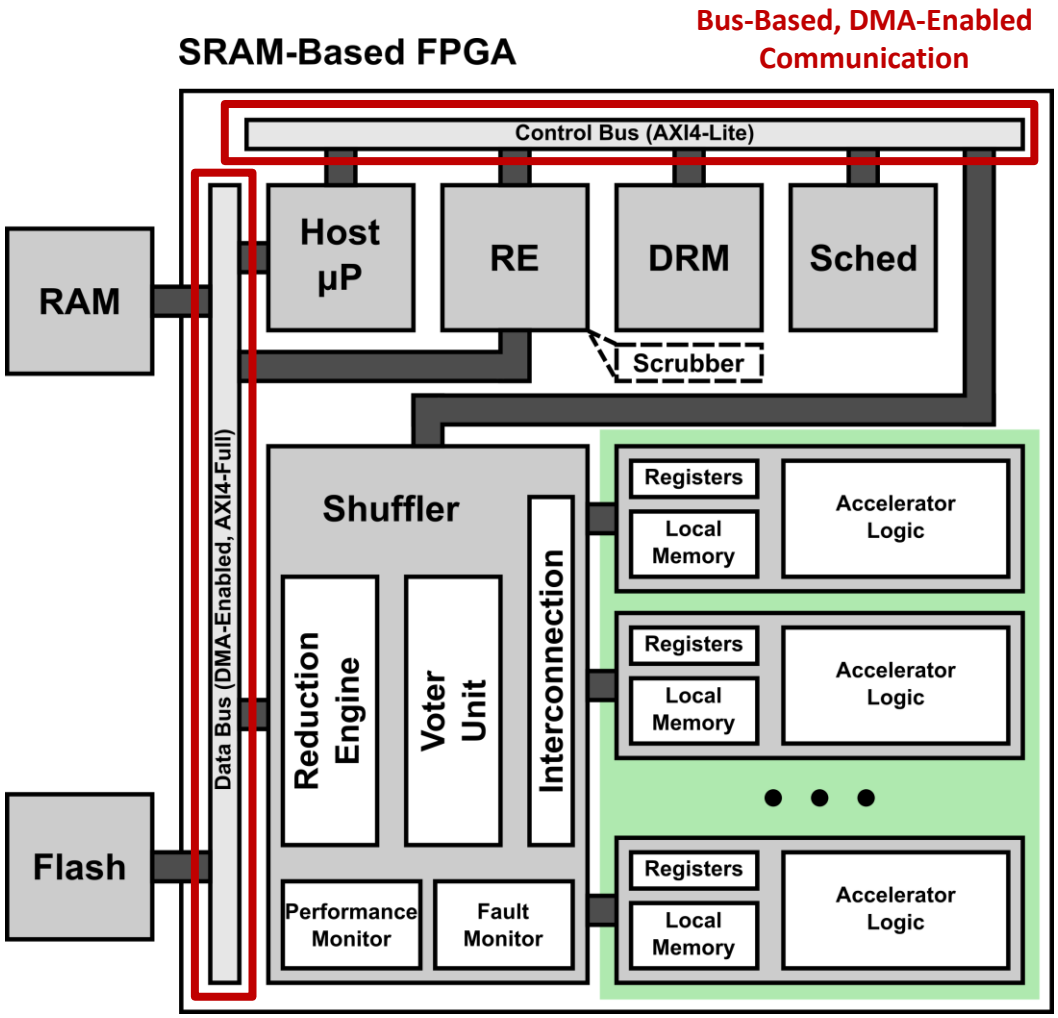

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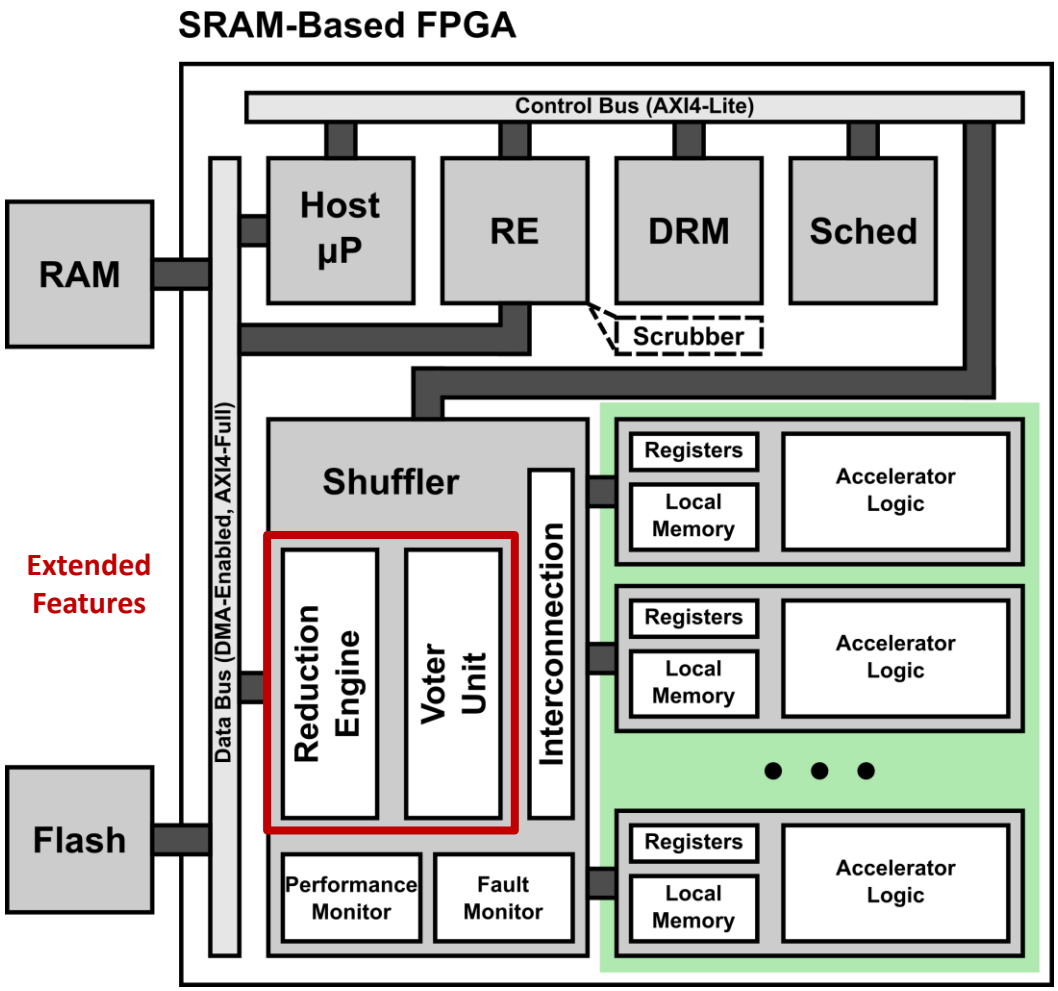

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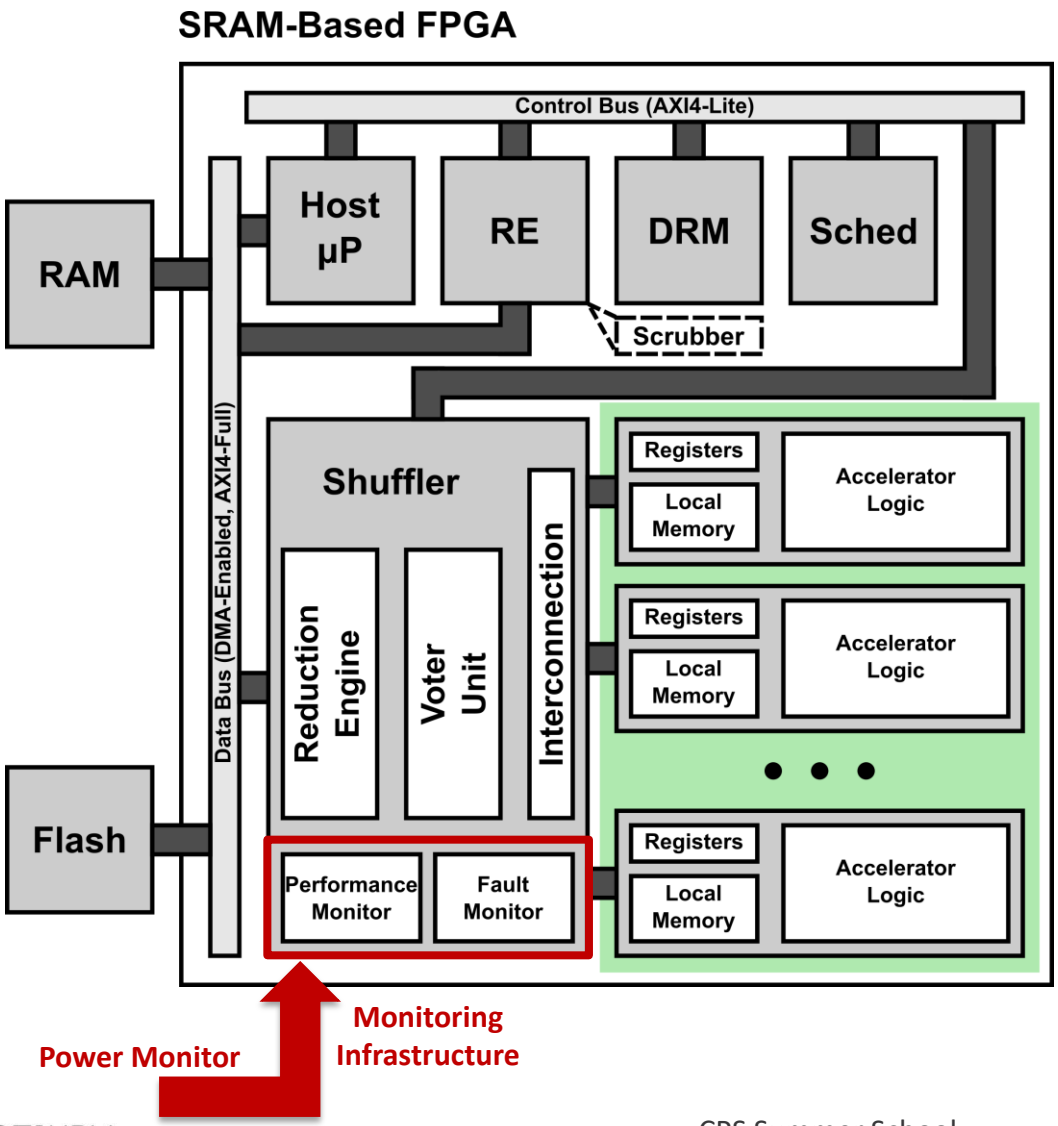
ARTICo^3 Architecture



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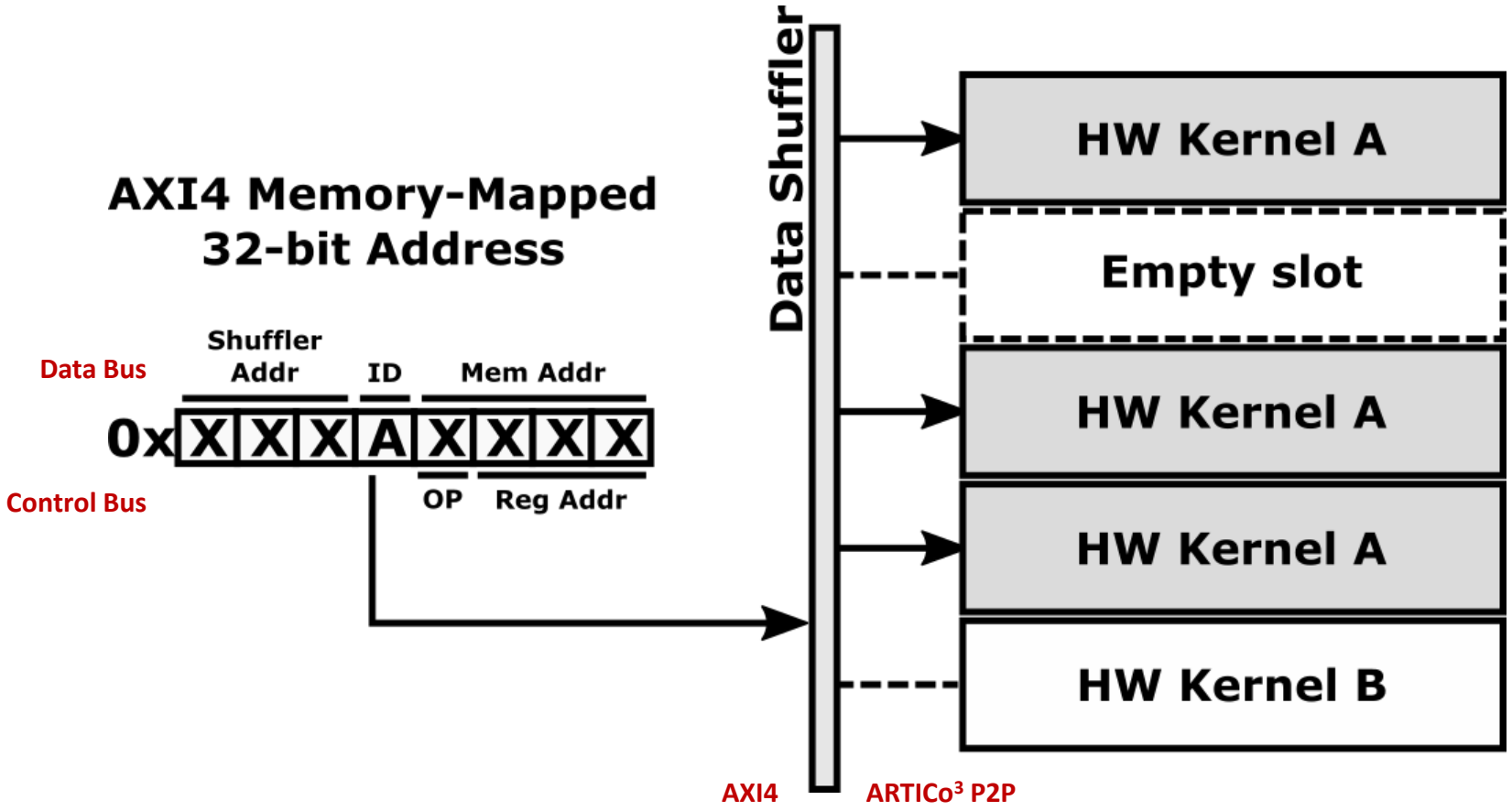
Accelerator Addressing



ARTICo^3-Compliant Accelerator Design

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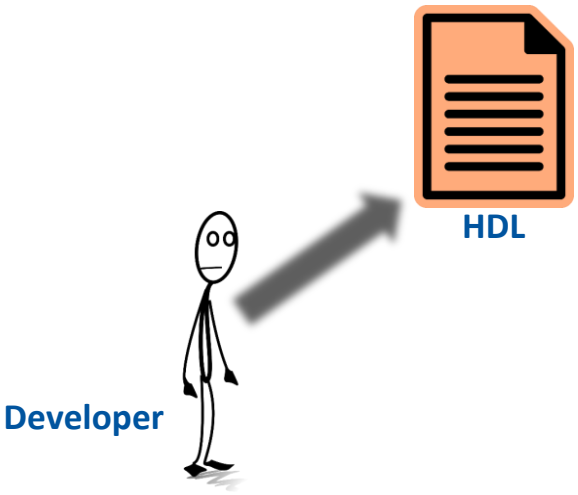

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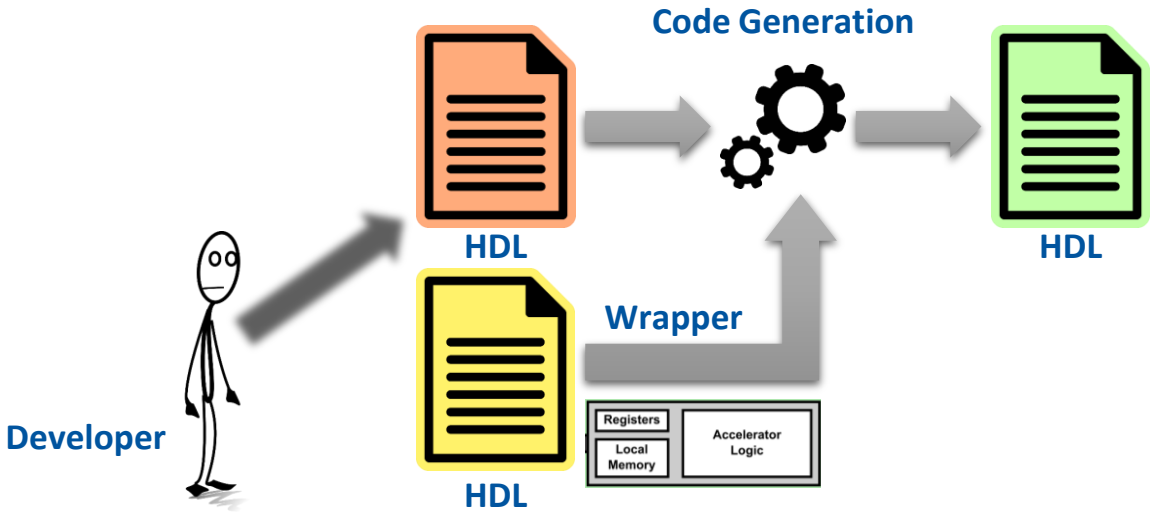

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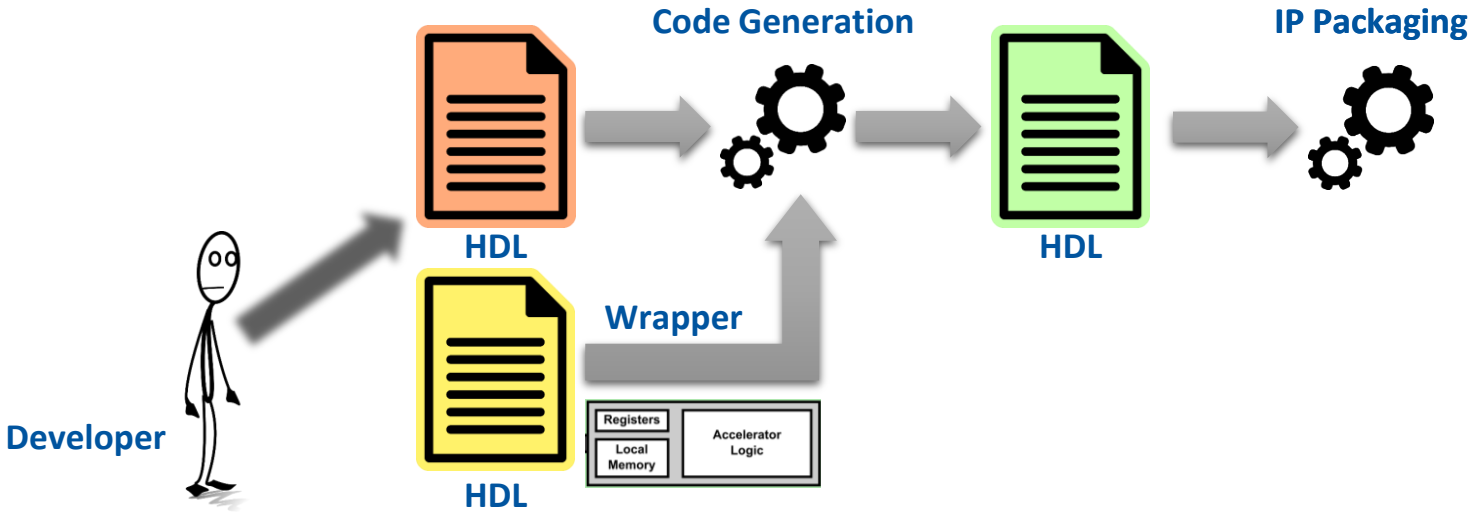

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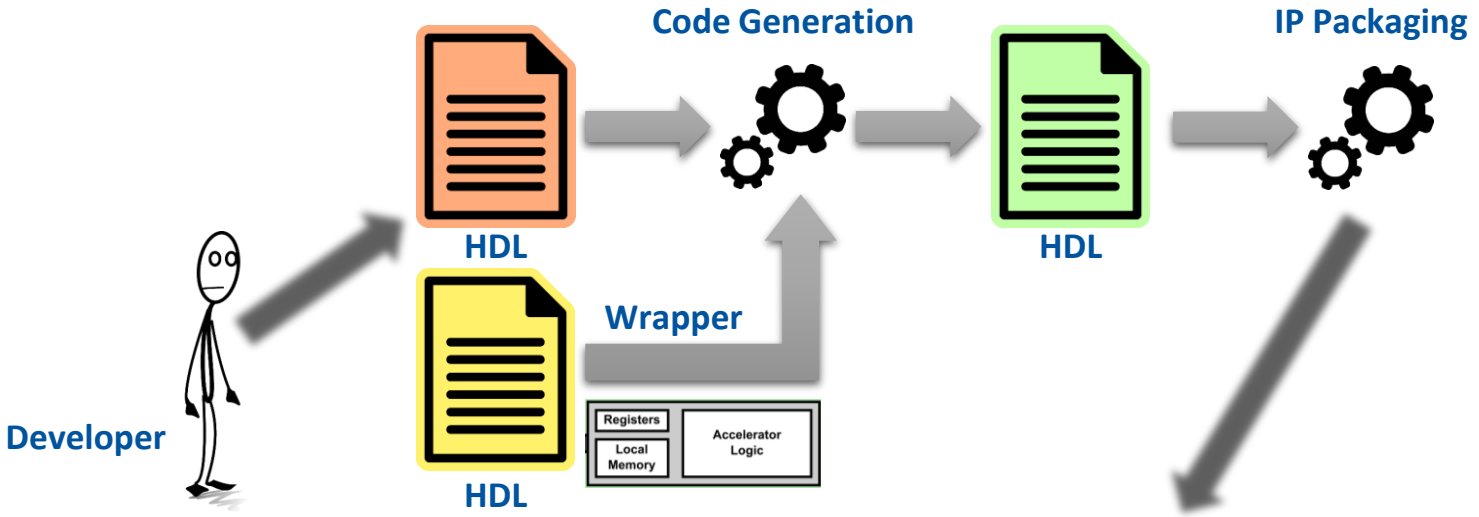

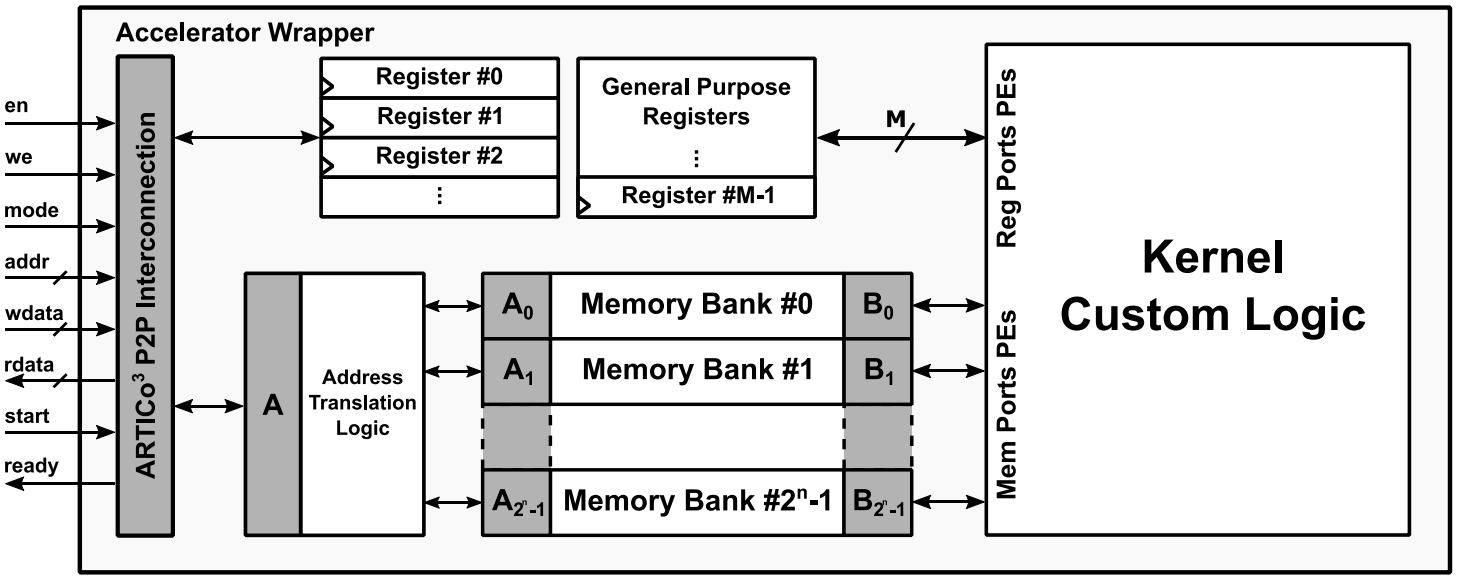

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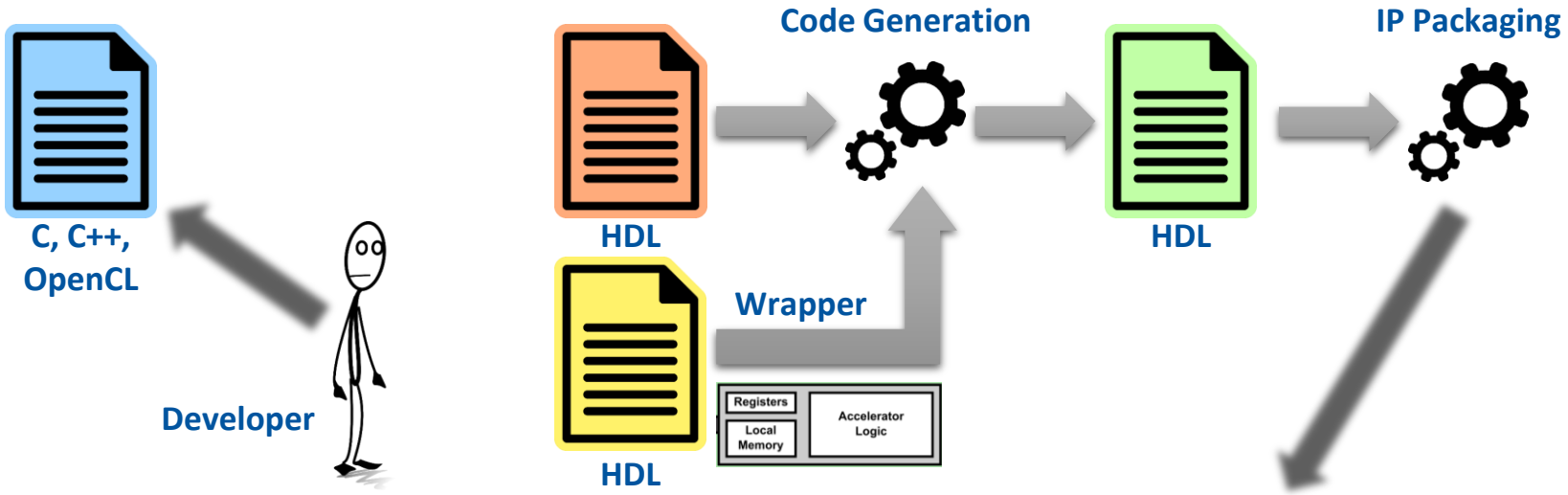

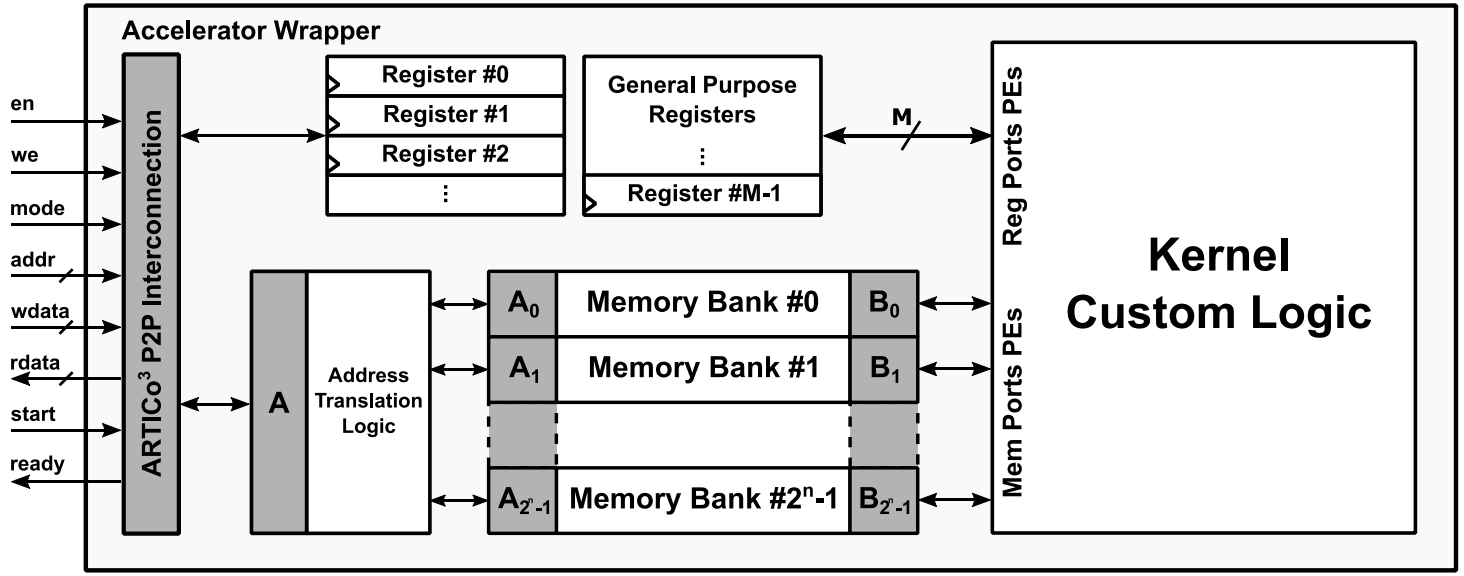

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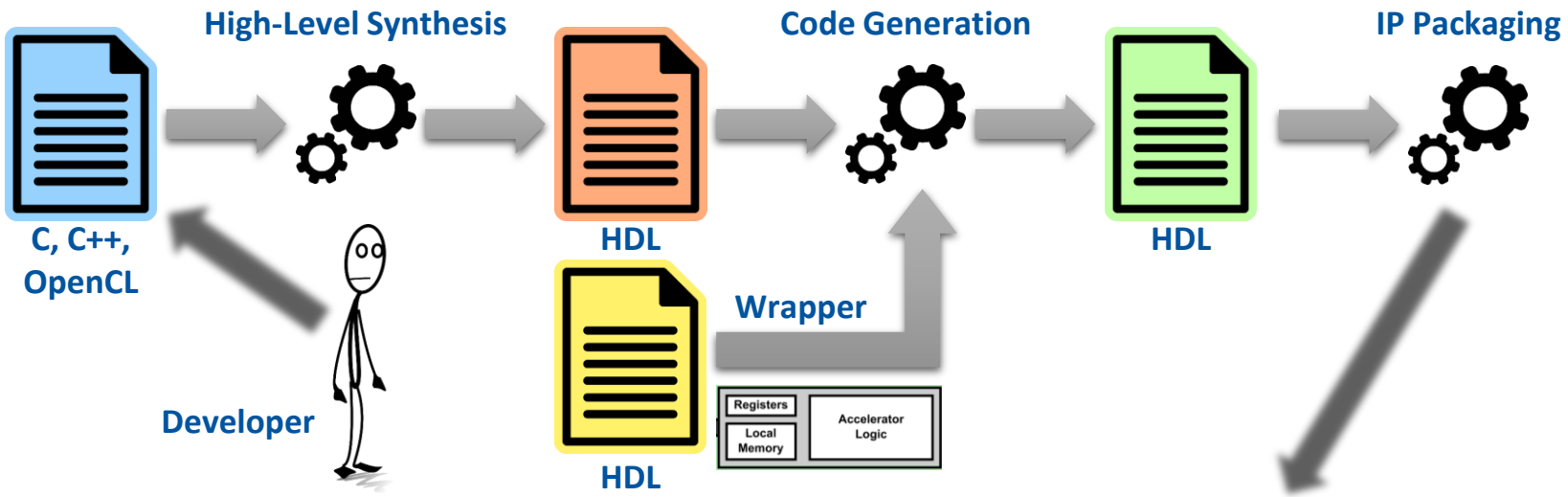
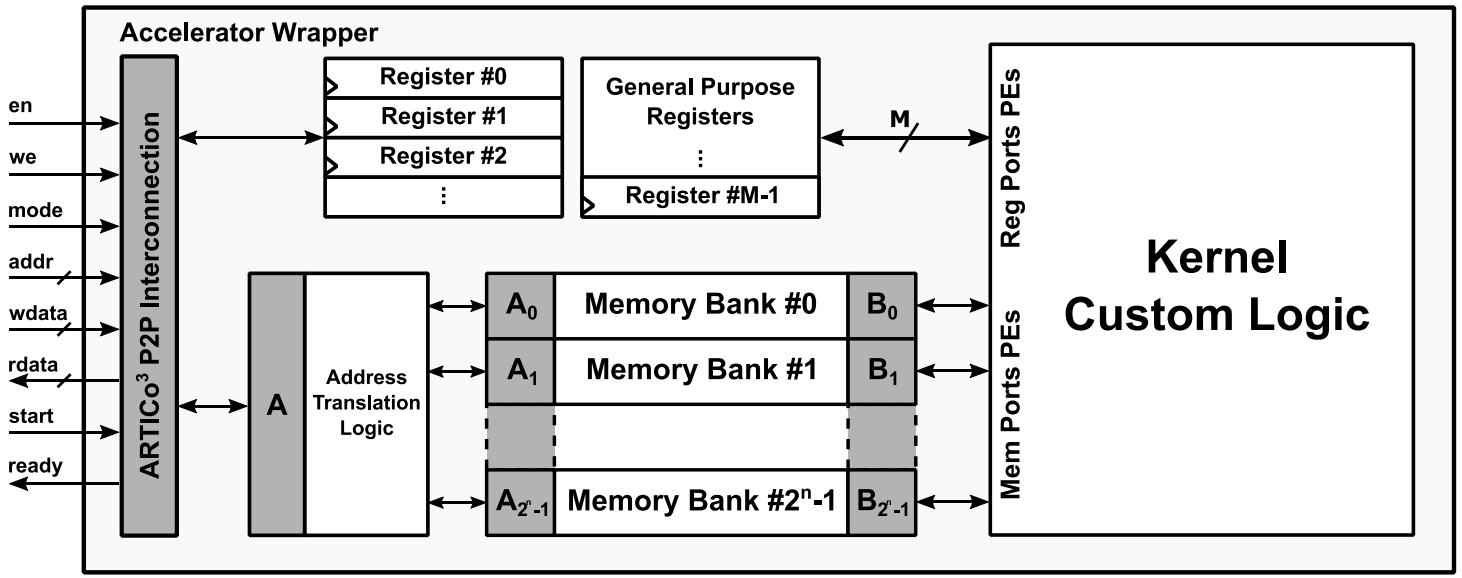
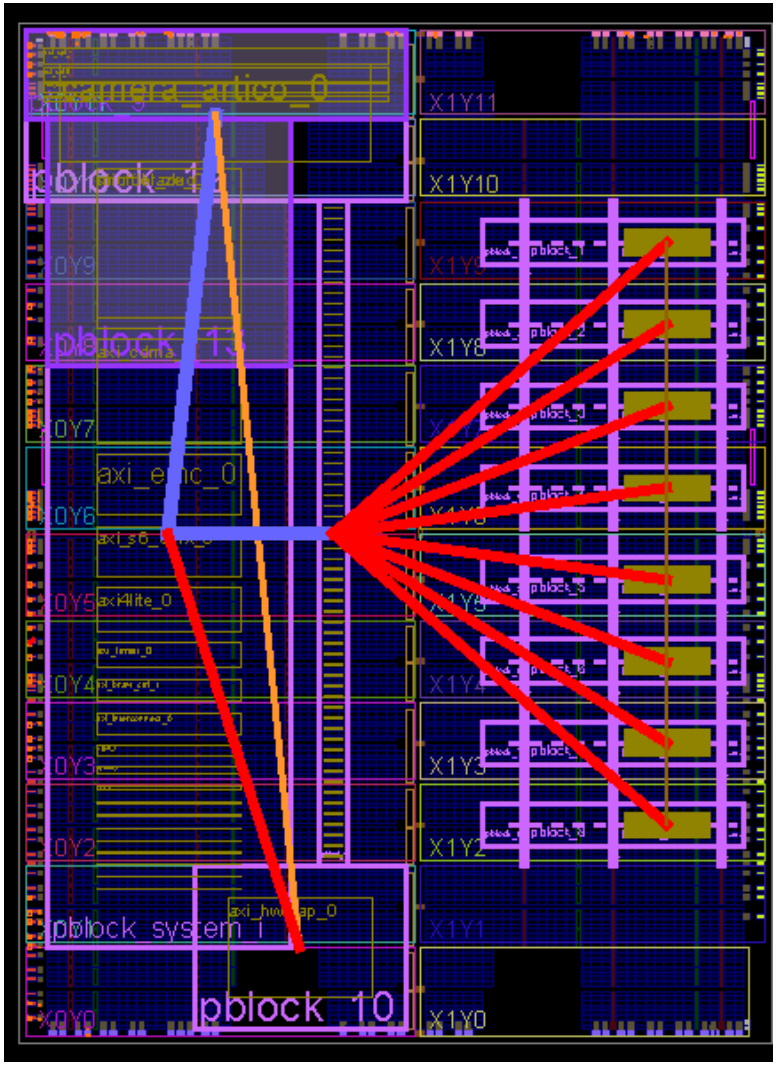




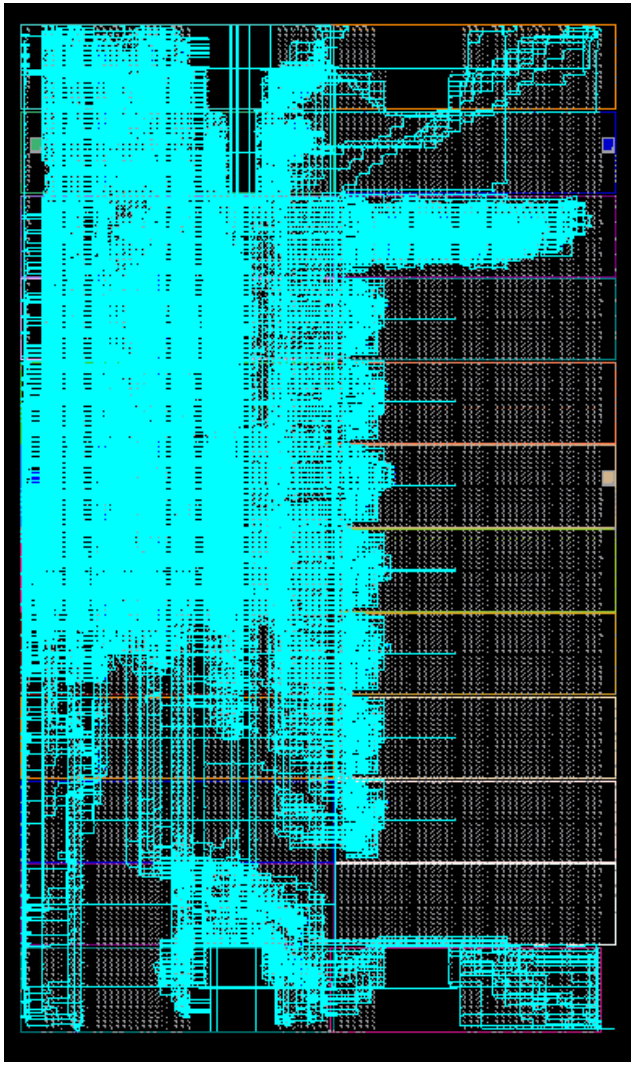
DPR-Compatible Floorplanning



Low-Level Constraints

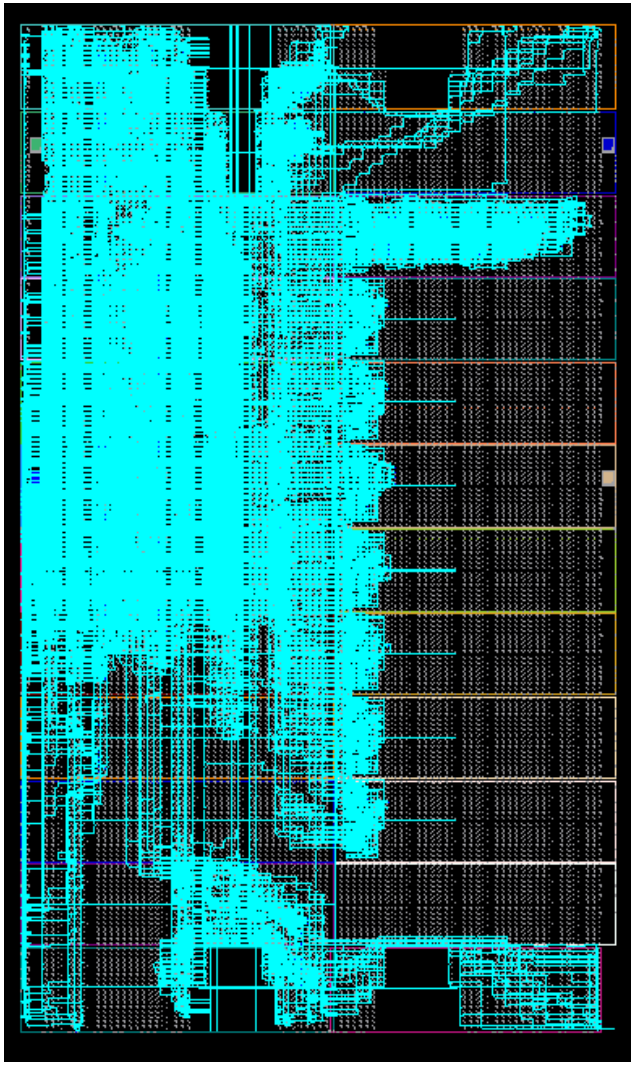
Design Placement

DPR-Compatible Floorplanning



- **Low-Level Constraints**
  - Design Placement
  - Design Routing

DPR-Compatible Floorplanning



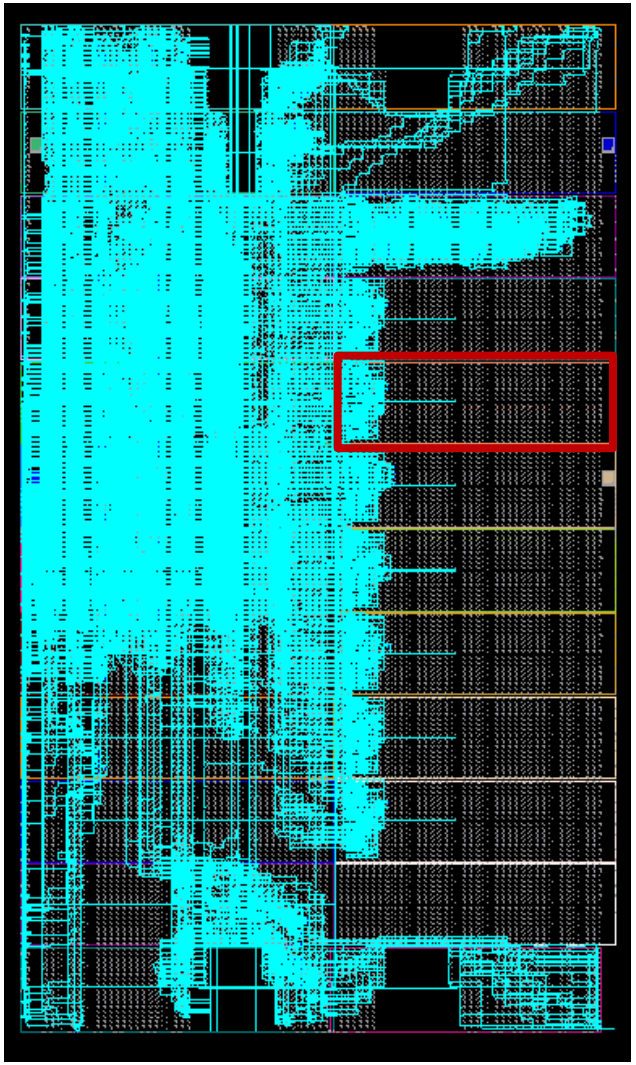
Low-Level Constraints

Design Placement

Design Routing

Technology Dependencies

DPR-Compatible Floorplanning



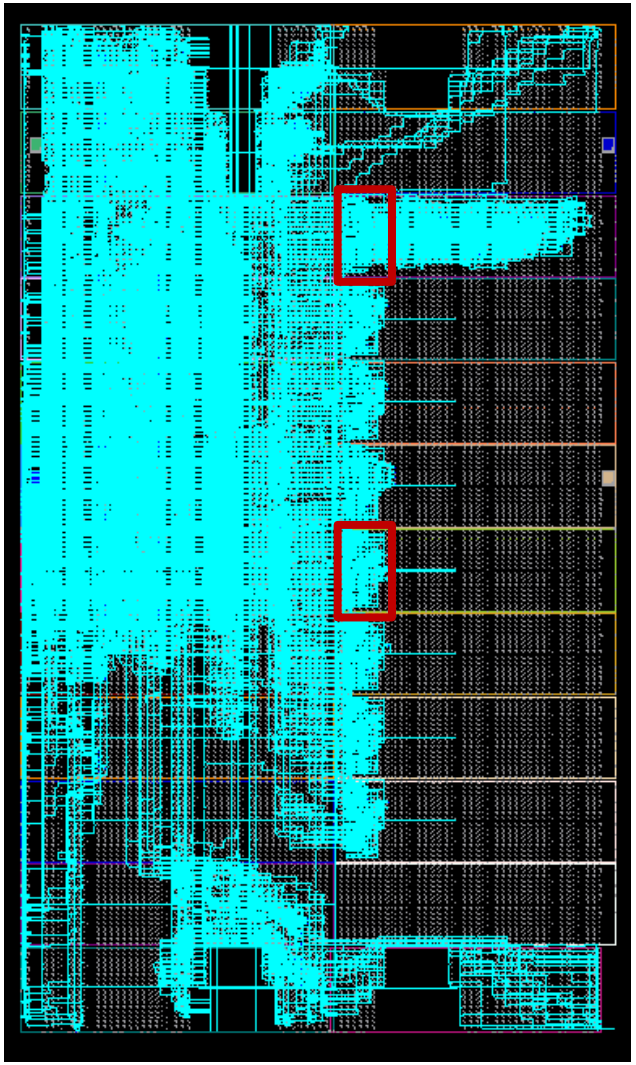
Low-Level Constraints

- Design Placement
- Design Routing

Technology Dependencies

- “Homogeneous” Fabric Layout

DPR-Compatible Floorplanning



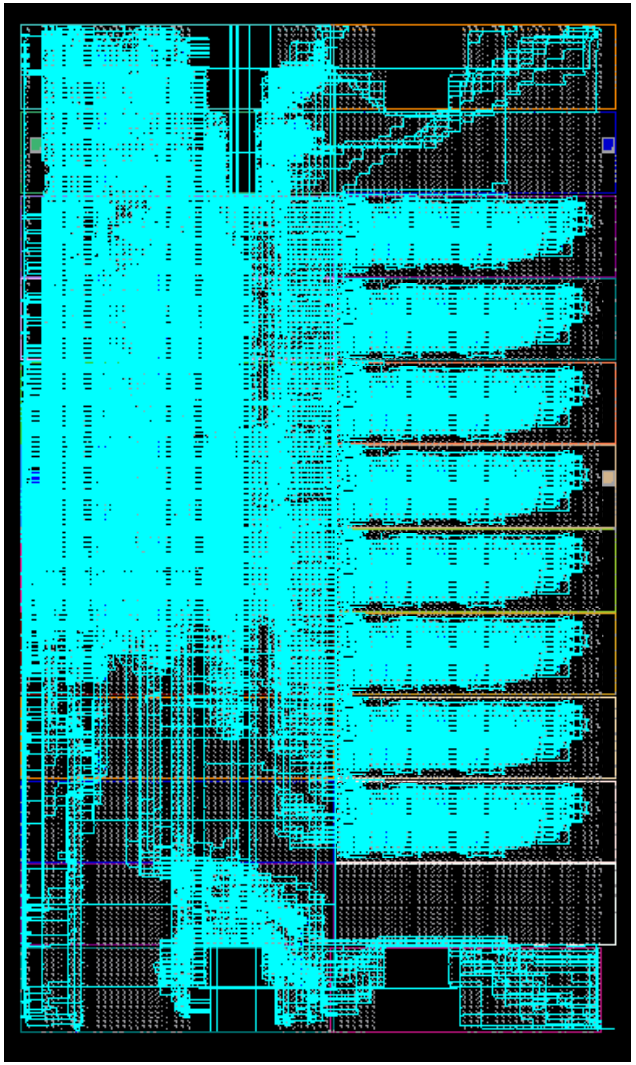
Low-Level Constraints

- Design Placement
- Design Routing

Technology Dependencies

- “Homogeneous” Fabric Layout
- Common Interfaces

DPR-Compatible Floorplanning



Low-Level Constraints

- Design Placement
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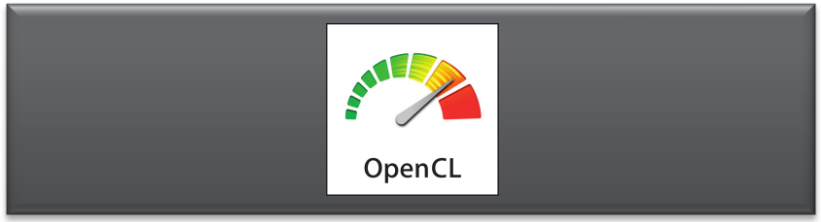
Technology Dependencies

- “Homogeneous” Fabric Layout
- Common Interfaces

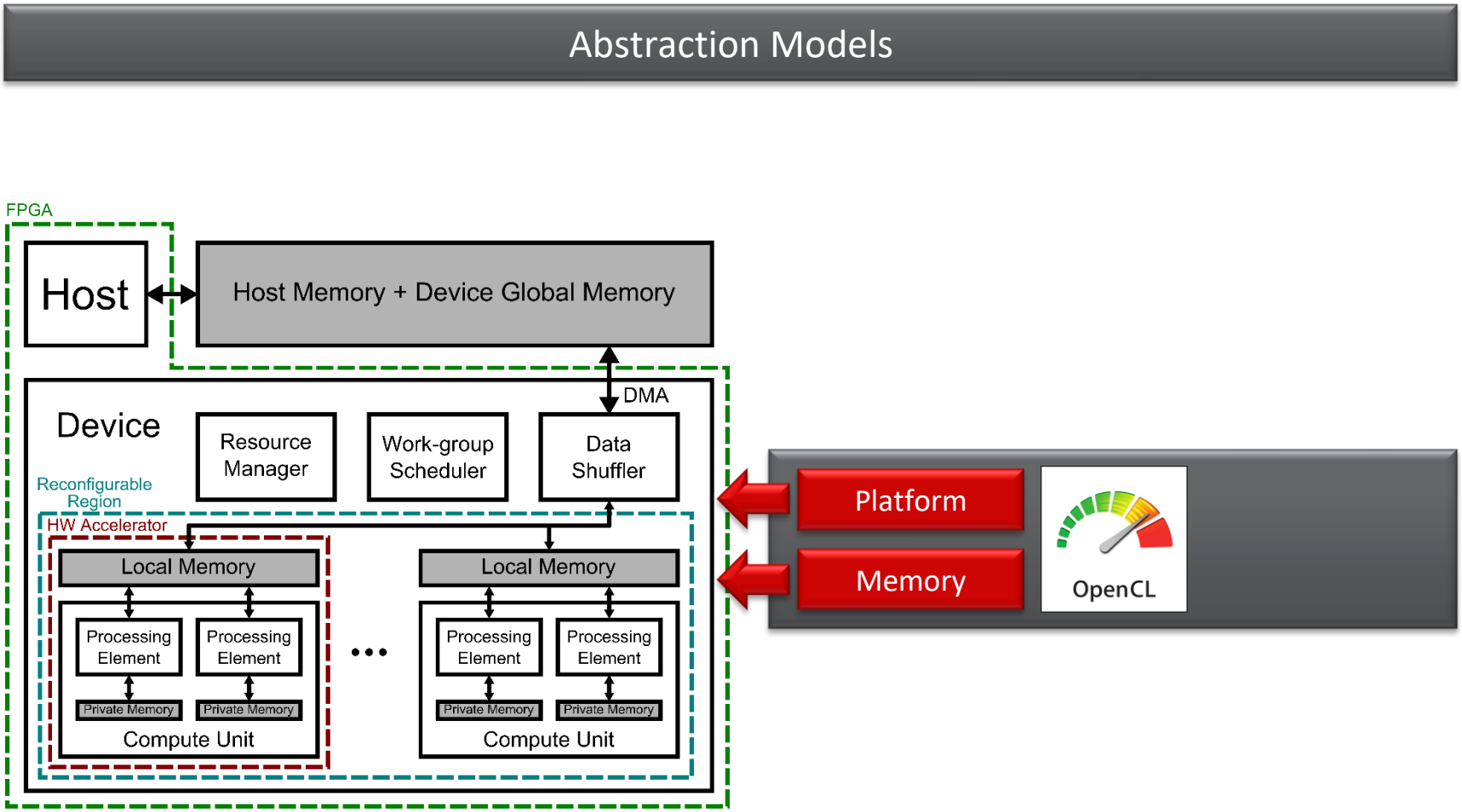
Hardware “Copy & Paste”

OpenCL-Like Runtime Framework

Abstraction Models



OpenCL-Like Runtime Framework



OpenCL-Like Runtime Framework

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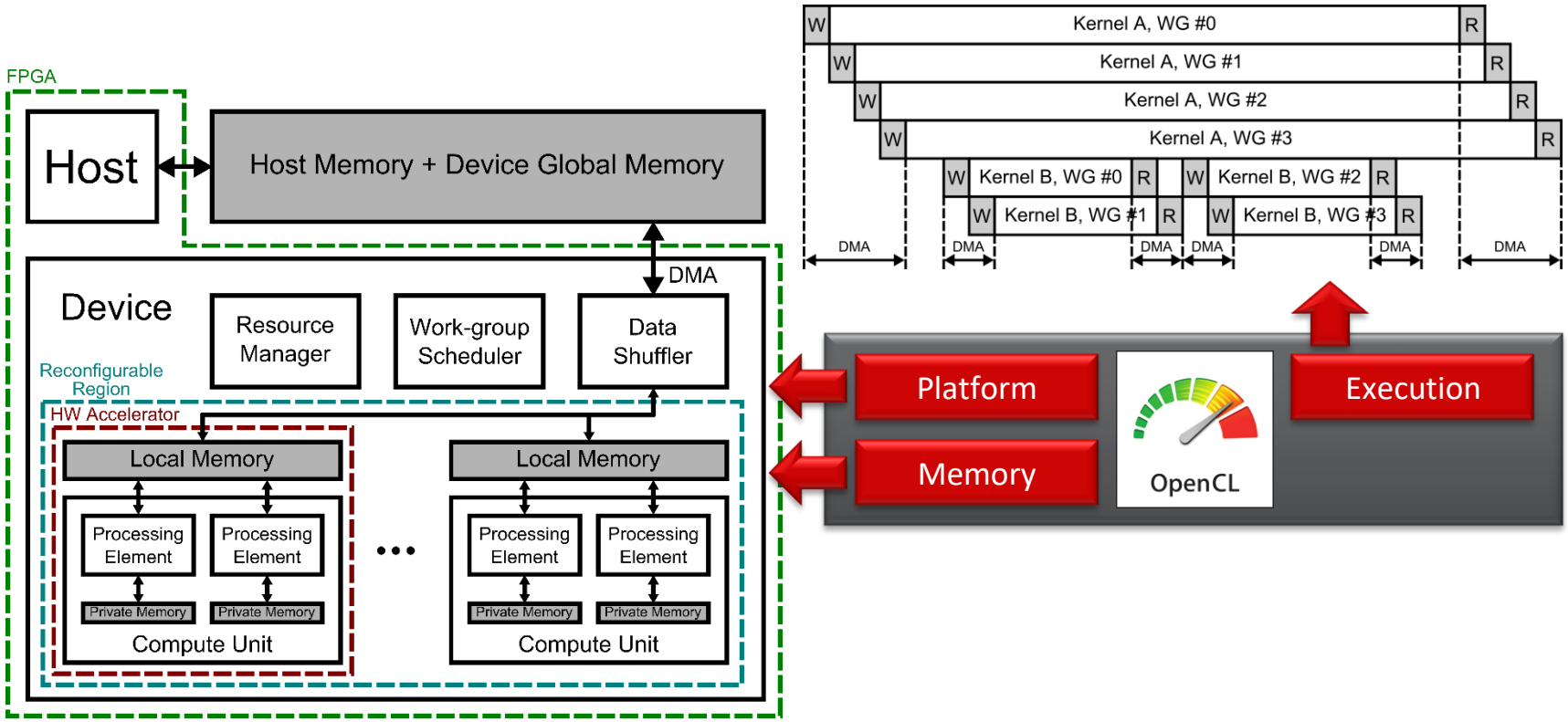

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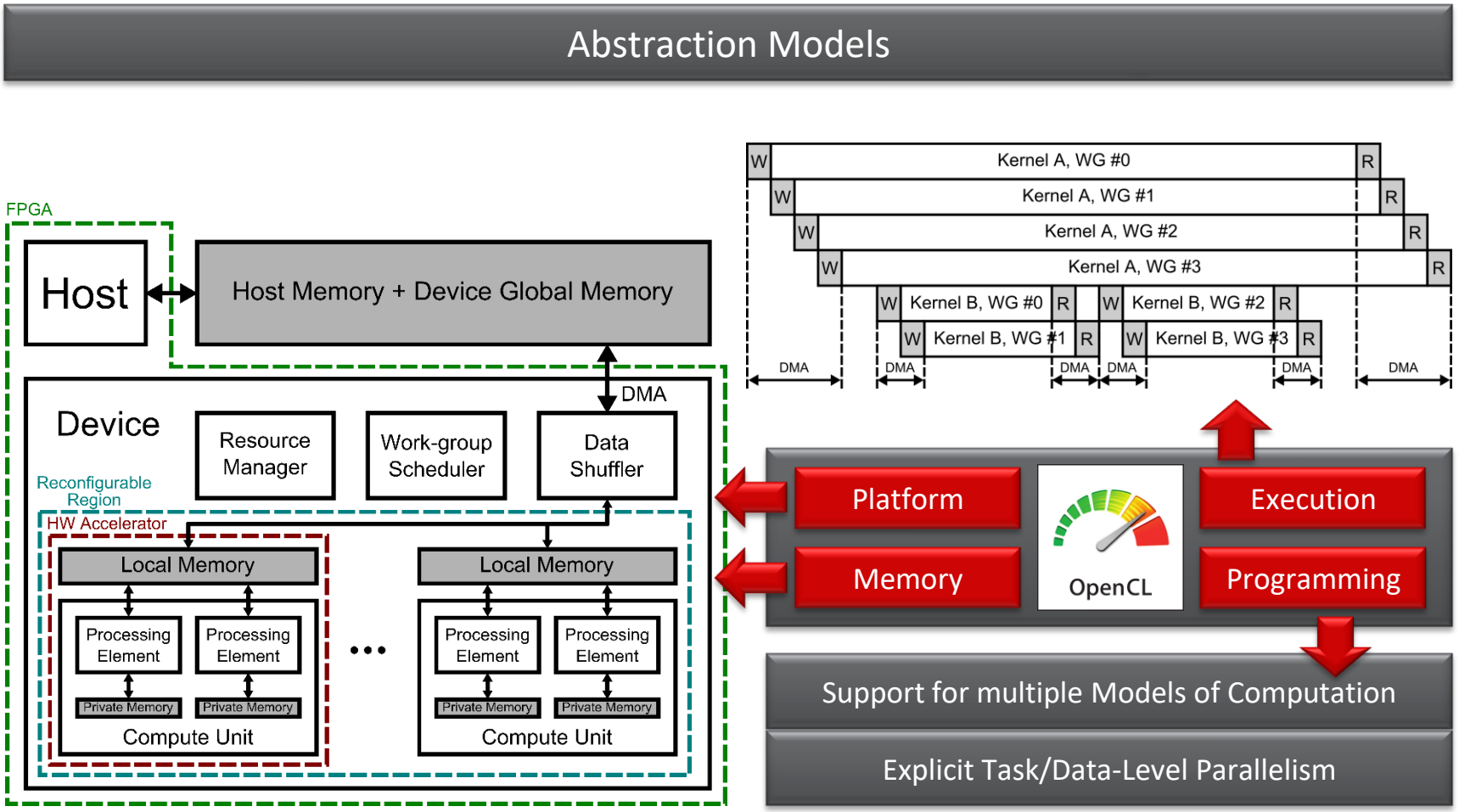

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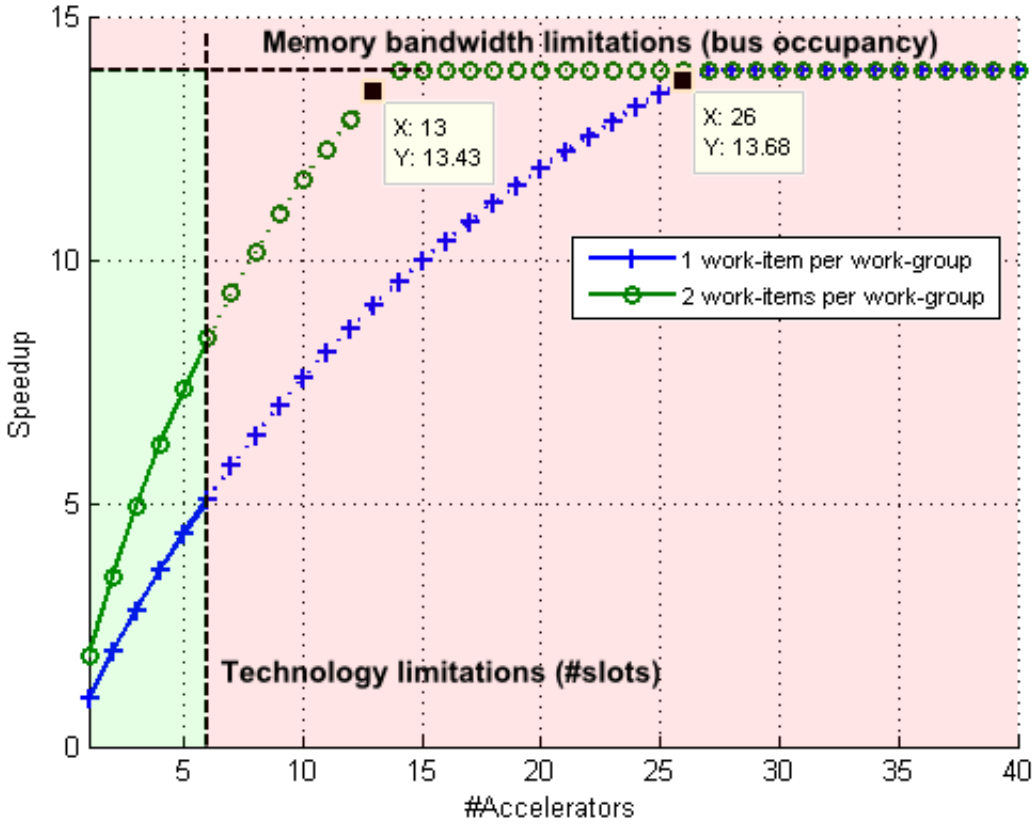

Tutorial Outline

- The ARTICo^3 repo
  - What is included in the release available in the VM?
  - Where are architecture, toolchain and runtime?
  - I don't know how to set up an embedded Linux, can I use ARTICo^3?
  - Open Source (not available yet!): **https://github.com/XXX/artico3.git**
- Demo applications
  - Dummy wait operation
    - Parallel execution of different hardware kernels
    - Debug mode (configuration and PMC registers dump)
  - Matrix multiplication (yes, we know…)
    - Scalable execution performance
    - Physical constraints and floorplanning
- How To…
  - …build an ARTICo^3 project from scratch?
  - …add new boards/devices?

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~~Tutorial~~ Fun time!

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