ANALOG AND MIXED-SIGNAL MICROELECTRONICS

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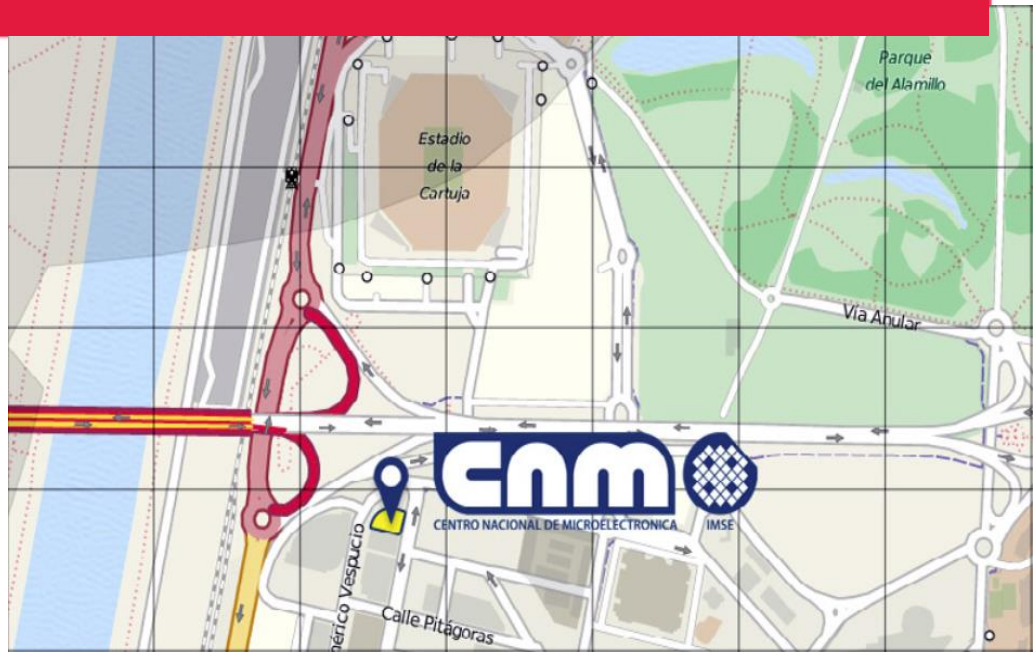
2. Ion Vornicu, PhD
3. Rafaella B. Fiorelli Martegani, PhD
4. Marco Trevisi
5. Belén Pérez Verdú, PhD
6. Jorge Fernández Berni, PhD
7. Manuel Carrasco Robles, PhD
8. Ricardo Carmona Galán, PhD
9. Manuel Moreno García
10. Ángel Rodríguez Vázquez, PhD
11. Juan Antonio Leñero Bardallo, PhD
12. Manuel Delgado Restituto, PhD
13. Rocío del Río Fernández, PhD
14. Fernando Medeiro Hidalgo, PhD

Not in the photo:
Óscar Guerra Vinuesa, PhD
Rafael Domínguez Castro, PhD

ANALOG AND MIXED-SIGNAL MICROELECTRONICS



ANALOG AND MIXED-SIGNAL MICROELECTRONICS

Head: Ángel Rodríguez Vázquez

14 Doctors + 4 PhD Students

- 2 Full Professors (US)
- 1 Scientist Researcher (CSIC)
- 4 Associate Professors (US)
- 1 Tenured Scientist (CSIC)
- 6 PostDocs

UNIVERSIDAD DE SEVILLA

CSIC
CONSEJO SUPERIOR DE INVESTIGACIONES CIENTÍFICAS

ANALOG AND MIXED-SIGNAL MICROELECTRONICS

Research Lines:

Design of AMS integrated circuits for sensing, signal conditioning and information processing in CMOS techs

① Design of ADCs and Mixed-Signal Interfaces

② Wireless Implantable and Wearable Intelligent Biosensor Devices

③ CMOS Smart Imagers and Vision Chips

④ Heterogeneous Sensory-Processing Systems and 3D Integration

European Training Network, H2020 (starting on October 1st)

ACHIEVE (AdvanCed Hardware/Software Components for Integrated/Embedded Vision SystEms)

List of participants

#	Participant Legal Name	Country
1	AGENCIA ESTATAL CONSEJO SUPERIOR DEINVESTIGACIONES CIENTIFICAS	Spain
2	Universite Clermont Auvergne	France
3	Universite Bourgogne Franche-Comte	France
4	UNIVERSITA DEGLI STUDI DI UDINE	Italy
5	UNIVERSIDADE DE COIMBRA	Portugal
6	UNIVERSITEIT GENT	Belgium
7	Specialised Imaging Ltd	United Kingdom

Information on partner organisations

Partner Organisation number	PIC Search PIC	Organisation legal name	Country	Academic Sector	Role of associated: Provide training	Role of associated: Host secondments	
1	939957355	FLIR Systems Trading Belgium FSTB	Belgium	No	No	Yes	
2		Prefixa Inc.	United States	No	Yes	Yes	
3	919815305	Kovilta Oy	Finland	No	No	Yes	
4	968729010	Nvidia Ltd	France	No	No	Yes	

Evaluation Summary Report

Evaluation Result

Total score: 95.00% (Threshold: 70/100.00)

Role and Commitment of key persons (including supervisors)	Ricardo Carmona-Galán (Coord. ETN), Tenured Scientist, 30% Rocío del Río Fernández (Coord. MSc) Associate Professor, 15% Jorge Fernández-Berni, Associate Professor, 15% Angel Rodríguez-Vázquez (Coord. PhD Prog) Full Professor, 10% Belén Pérez-Verdú (Dean Faculty of Physics), Full Professor, 10%

MASTER IN MICROELECTRONICS: DESIGN AND APPLICATIONS OF MICRO/NANOSCALE SYSTEMS

Título de Máster Universitario verificado por la ANECA y publicado su carácter oficial en el BOE Nº 236 de 29/09/2010.
Inscrito en el Registro de Universidades, Centros y Títulos con el nº 4312169.
Plan de Estudios aprobado por la Resolución de 20 de Julio de 2011 de la Universidad de Sevilla, publicado en el BOE Núm. 259 de 27 de octubre de 2011.

COURSES

- Micro- and Nano-Devices and Technologies
- Design of Analog, Digital, Mixed-Signal and RF (AMS/RF) Integrated Circuits
- Applications, Systems and Techniques for Information Processing
- Design Methodologies and CAD Tools
- Wireless Transceivers: Standards, Techniques and Architectures
- Circuit Design for RF Front-End
- Electromagnetic Fundamentals for RF Design
- Sensors in Integrated Technologies
- Bio-Inspired Processing: Algorithms and Circuits
- Neuromorphic and Fuzzy Systems: Applications and Case Studies
- Test and Design-for-Test
- Advanced Design Techniques
- Emerging Technologies
- Work Placement in Companies and/or Research Centers
- Master's Thesis

NEWS

- PHASE 3 FOR PRE-REGISTRATION in the Master for the academic year 2017-18 will be opened FROM SEPTEMBER 28th TO OCTOBER 2nd. For more details, please check the info in the section "Admission".
- The ANNOUNCEMENTS page includes "Job offers, scholarships, etc.".

EXPON@US

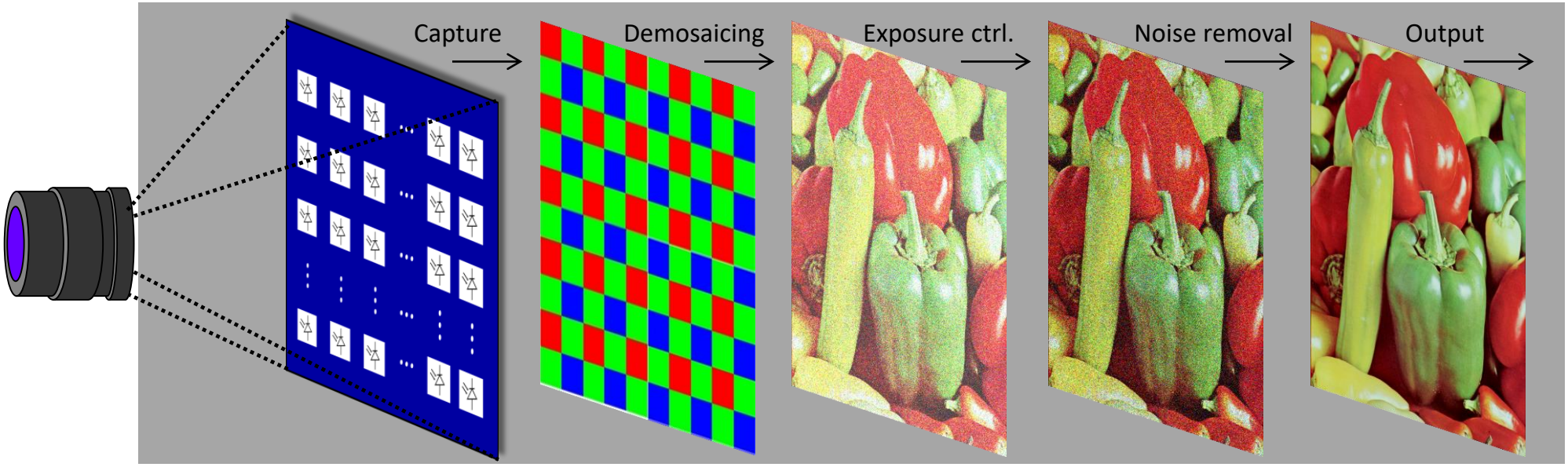
http://www.mastermicroelectronica.us.es/en/

Jorge Fernández-Berni, PhD

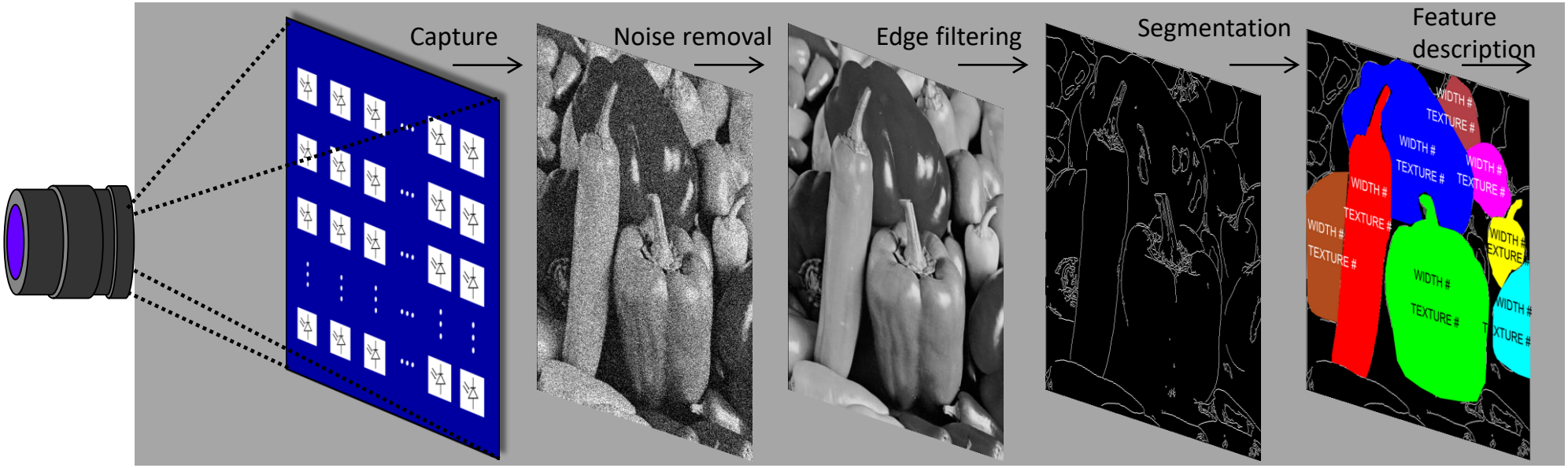
jfernandez8@us.es

Concepts of Imaging and Vision Sensors

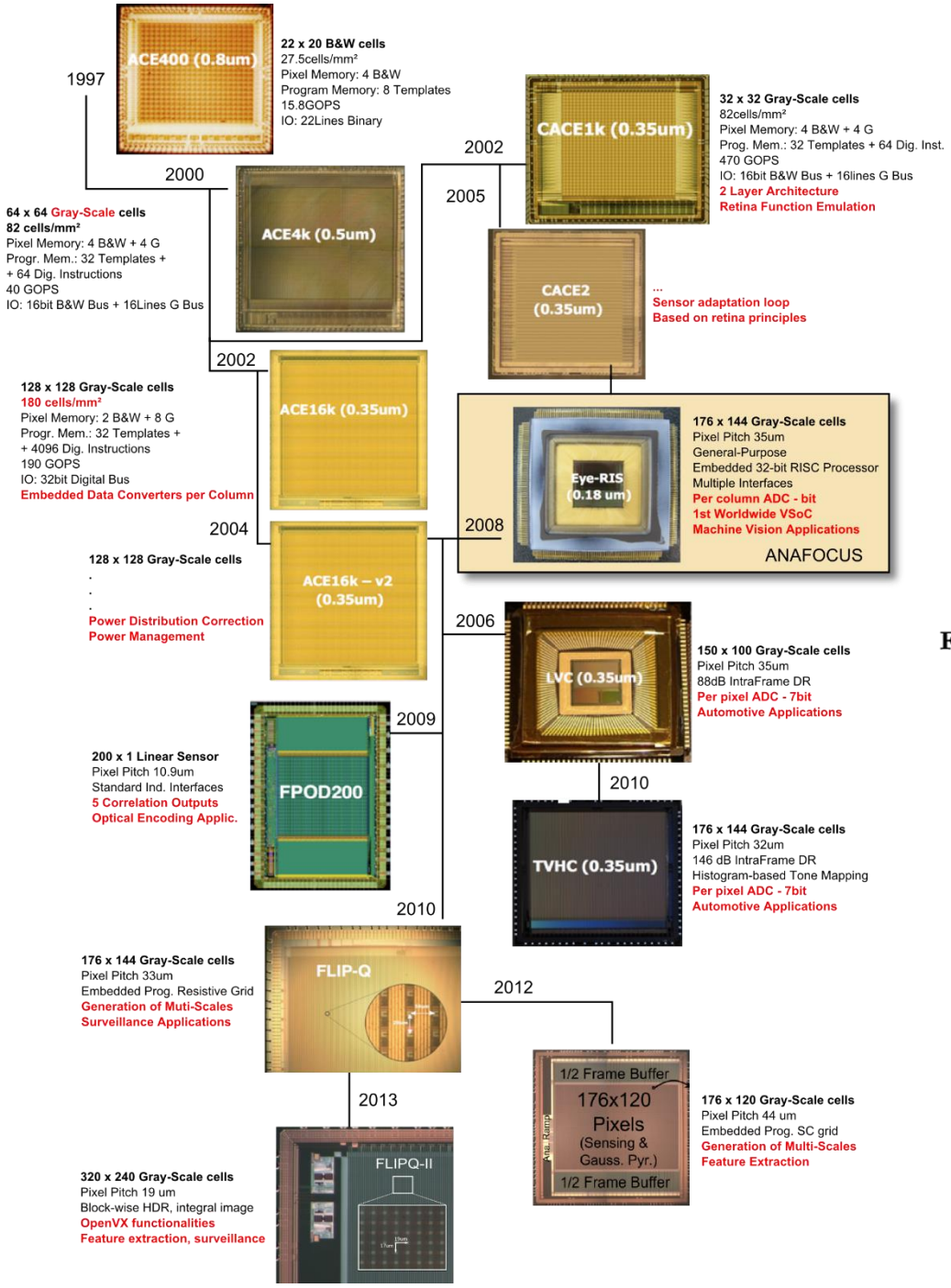
IMAGING Main objective: image quality

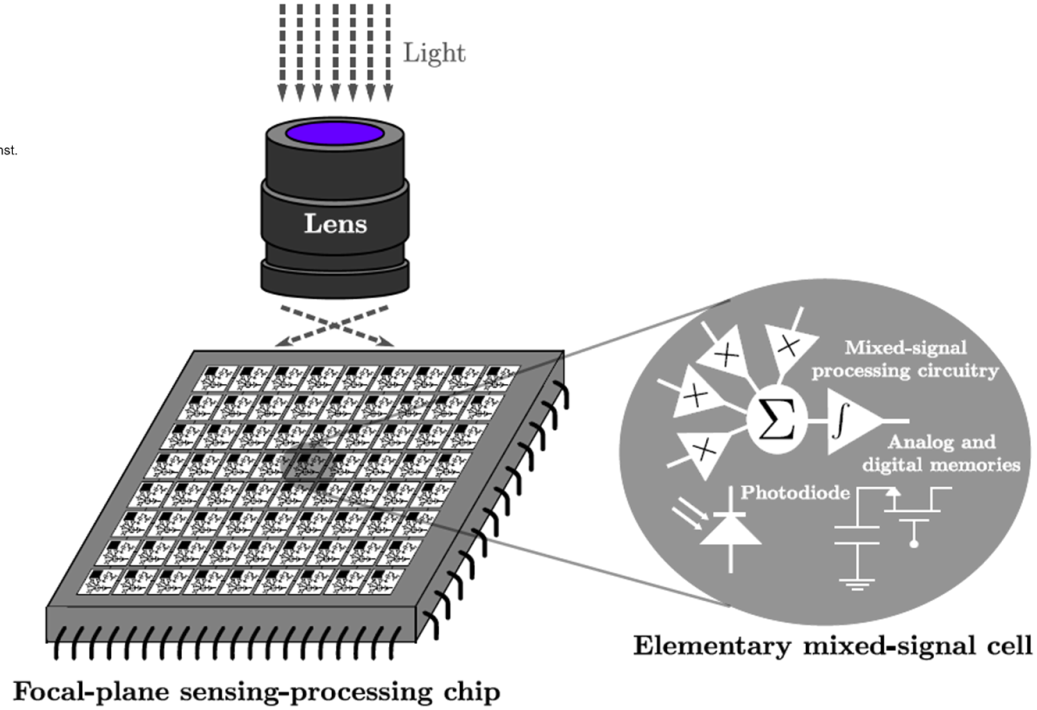


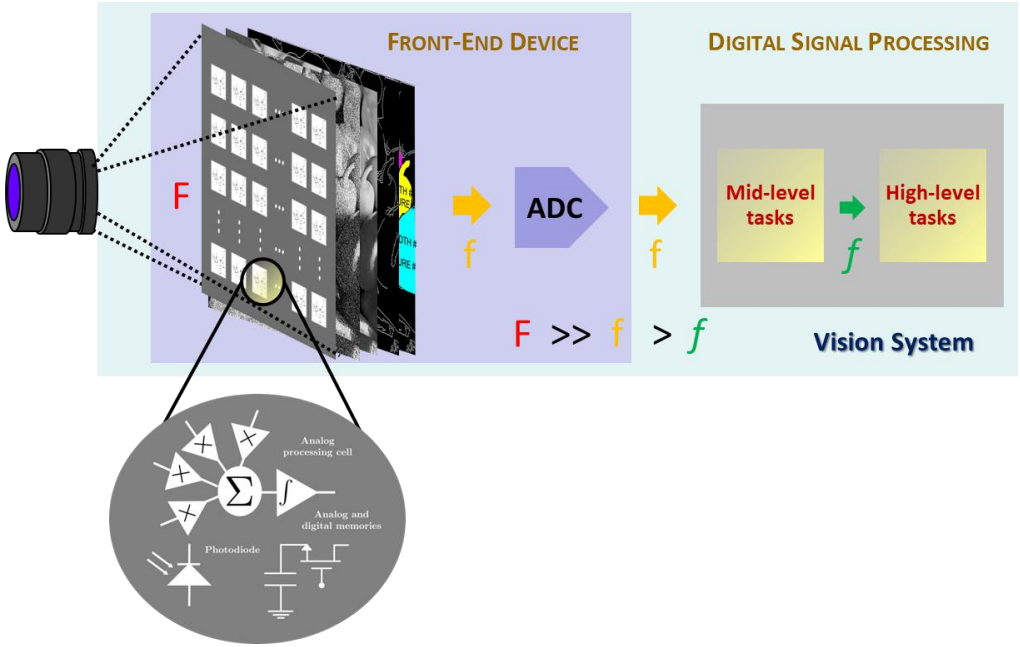
VISION Main objective: scene understanding



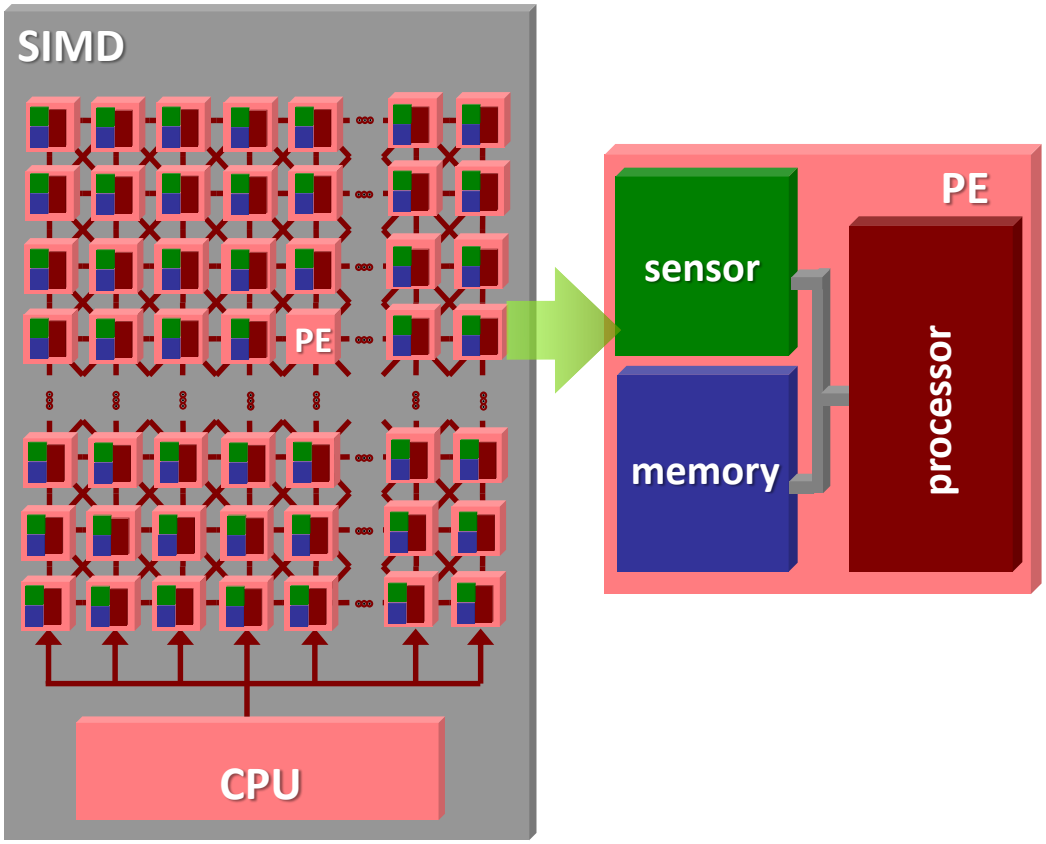
Vision chips based on focal plane processing

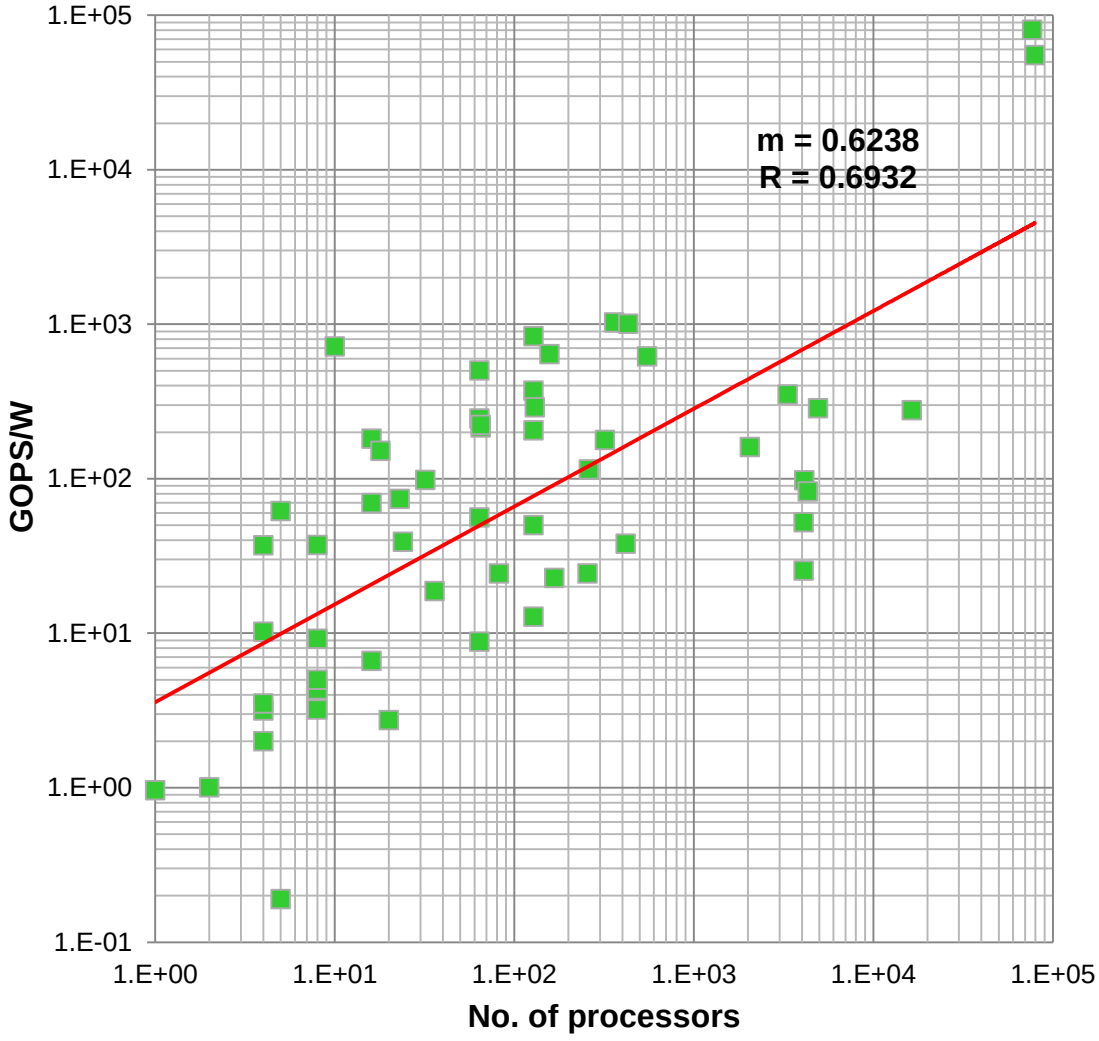






Power efficiency through architecture

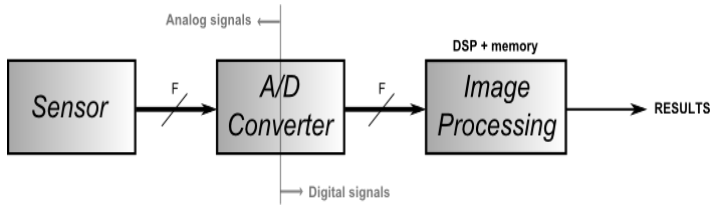




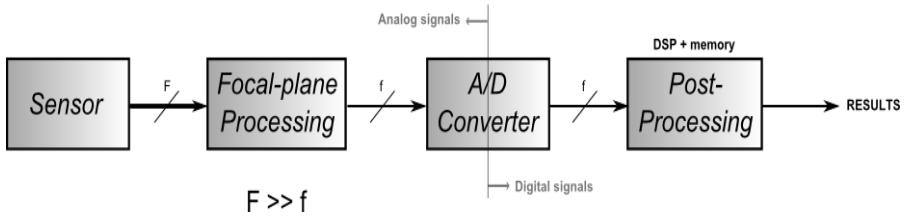
- **Distributed processing is more efficient than conventional serialized architectures**
- **Parallelizing computing resources:**
  - a) **meets otherwise intractable timing requirements (overcoming Amdahl's law)**
  - b) **reduces the power consumption overhead due to data conversion and transfer**

Hierarchical vision processing architecture

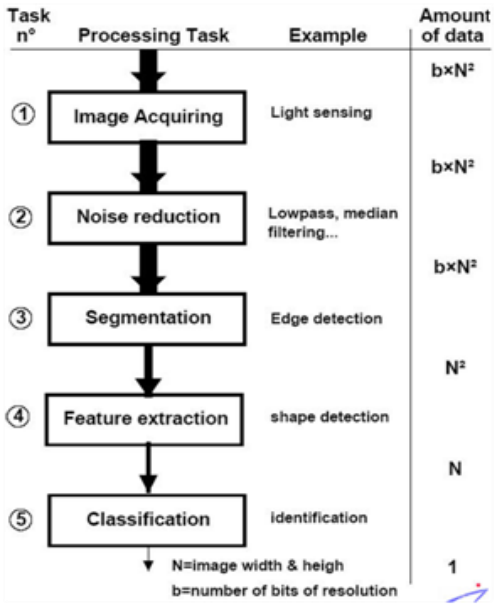
Conventional image processing chain

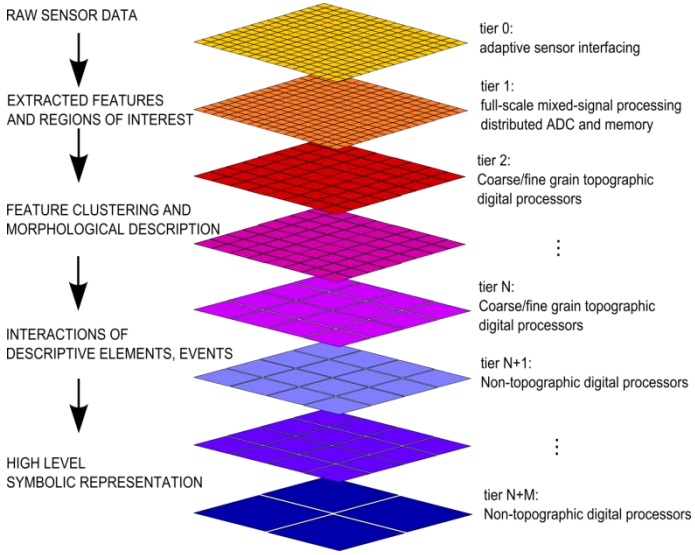


Bioinspired/hierarchical approach

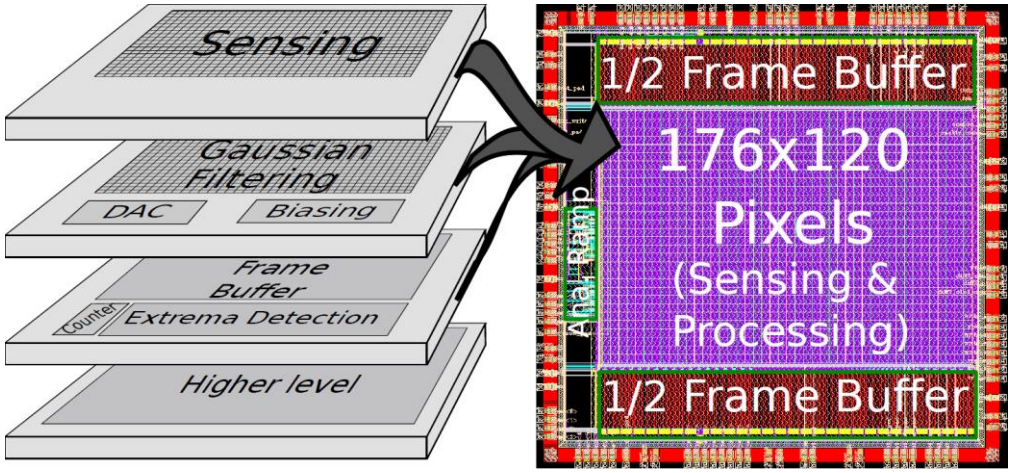


Functional / physical 3D mapping



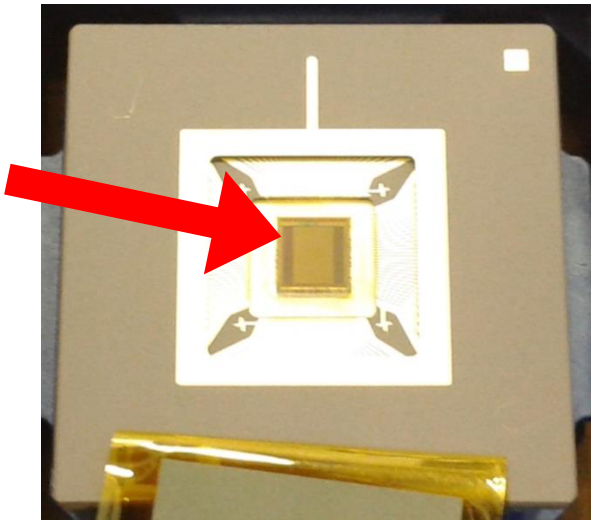


3D architecture emulation



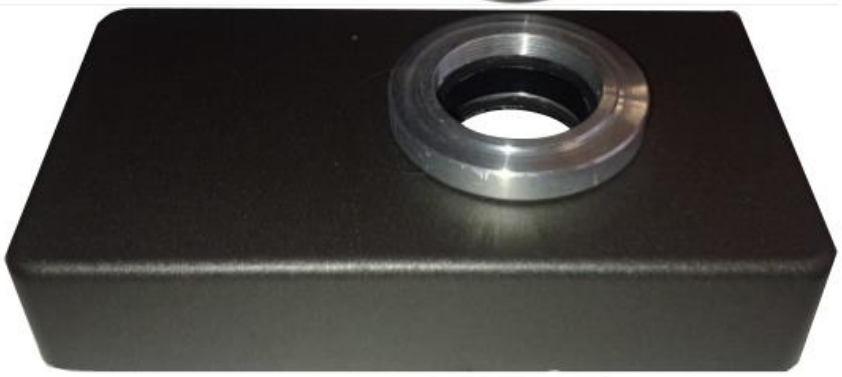
[IEEE JETCAS 2012]

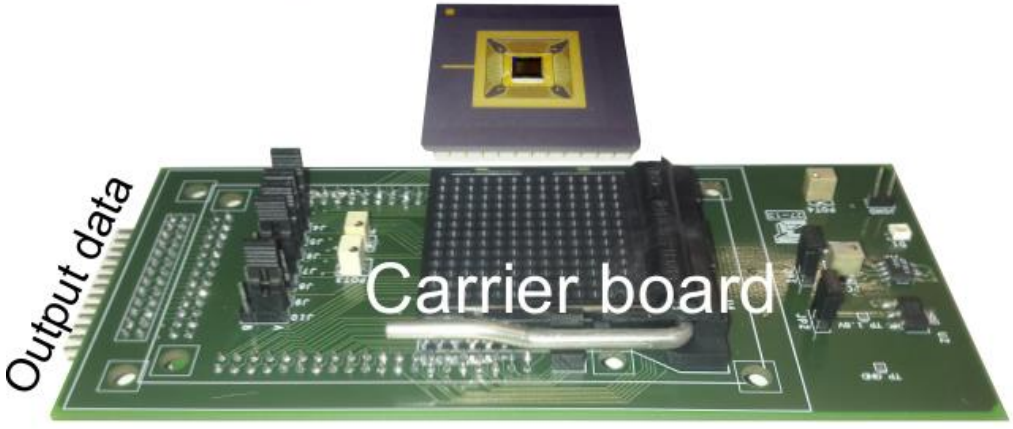
Technology	CMOS 180nm
No. pixels	176×120
No. PE's	88×60
Chip area	5×5 mm^2
Cell area	44×44 mm^2
Power	75nW/px @30fps
Min. filter	σ = 0.48



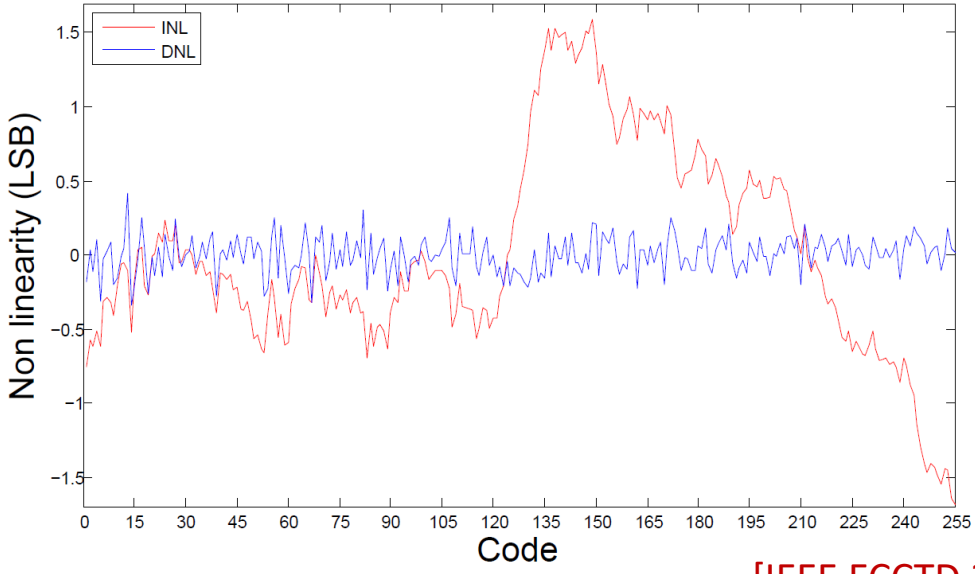
Hierarchical vision processing architecture

Test and application development setup



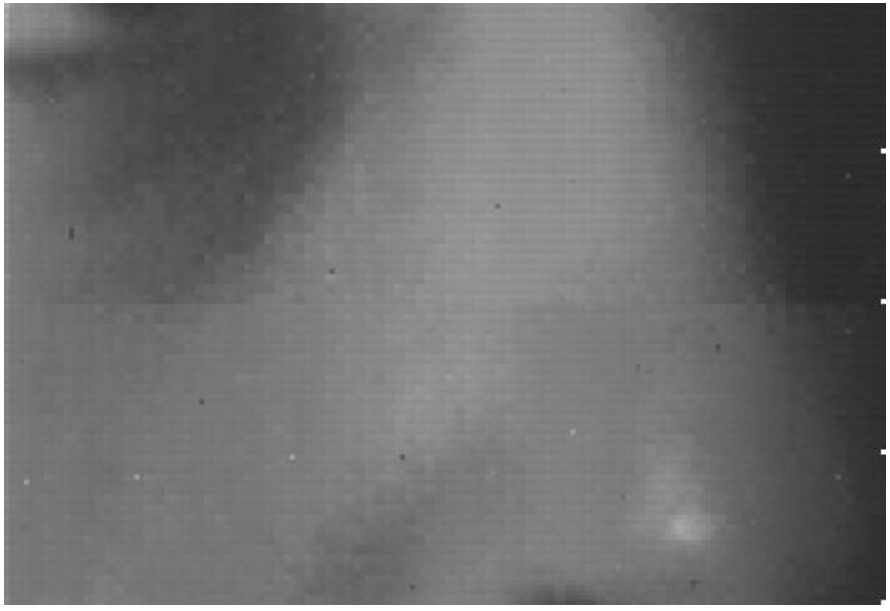


Fully-parallel conversion with ramp ADC

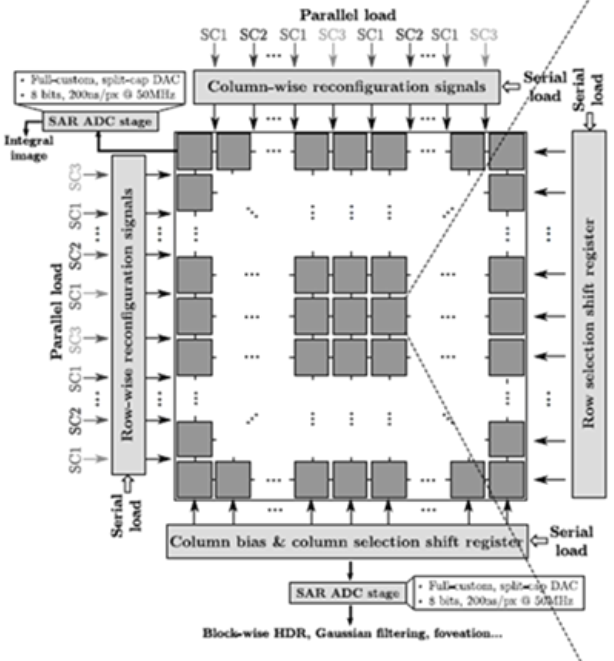


[IEEE ECCTD 2013]

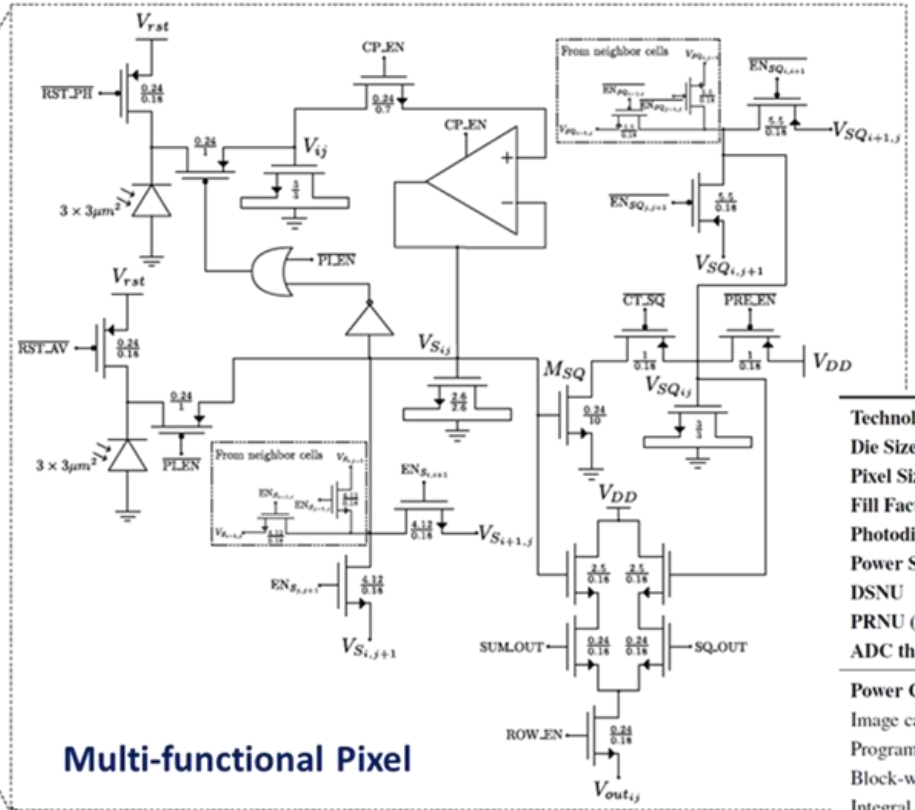
Image capture and step-by-step Gaussian filtering



Power efficiency through image representation



Chip Floorplan



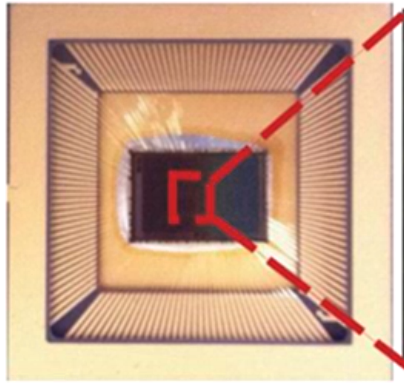
Multi-functional Pixel

EMBEDDED FUNCTIONALITY

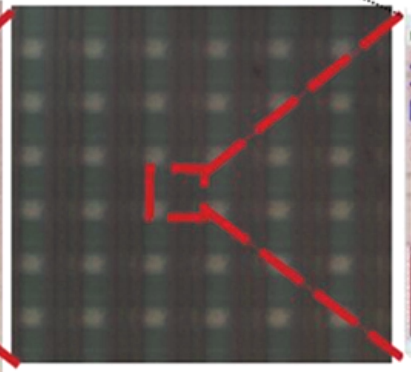
- Reconfigurable concurrent dual sensing
- Integral image computation
- Energy-based representation
- Reduced kernel filtering
- Programmable obfuscation

Technology	0.18 µm 1.8 V 1P6M CMOS process
Die Size (with Pads)	7.5 mm × 5 mm
Pixel Size	19.59 µm × 17 µm
Fill Factor	5.4%
Photodiode Type	n-well/p-substrate
Power Supply	3.3 V (pads), 1.8 V (core)
DSNU	1.7%
PRNU (50% Signal Range)	3.5%
ADC throughput	5 MSa/s (200 ns/Sa)
Power Consumption at 30 fps	
Image capture	42.6 mW
Programmable pixelation	43.8 mW
Block-wise HDR	42.6 mW
Integral imaging	55.2 mW
Gaussian filtering	43.1 mW

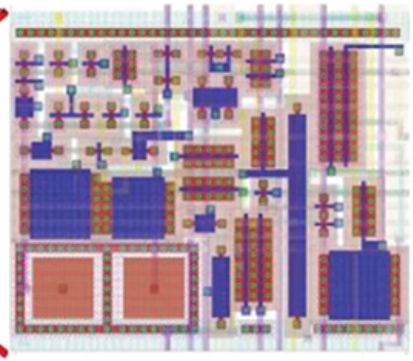
PGA144 Chip Package



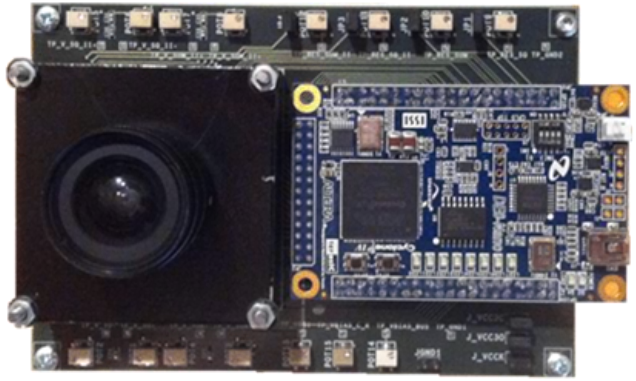
Micro-photograph



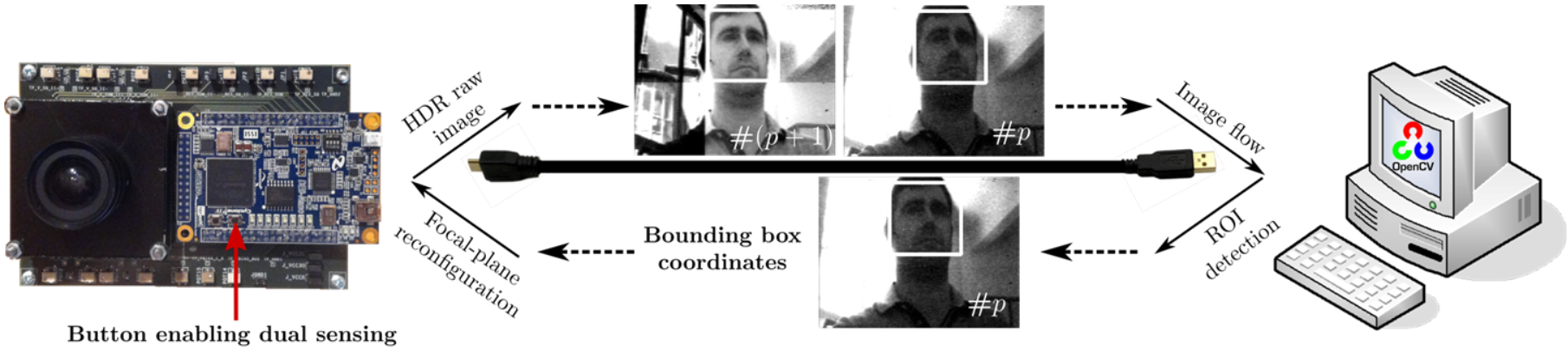
Pixel Layout



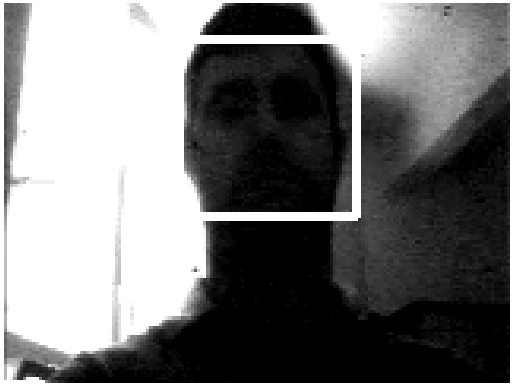
FPGA-based test system



Power efficiency through image representation



FACE TRACKING

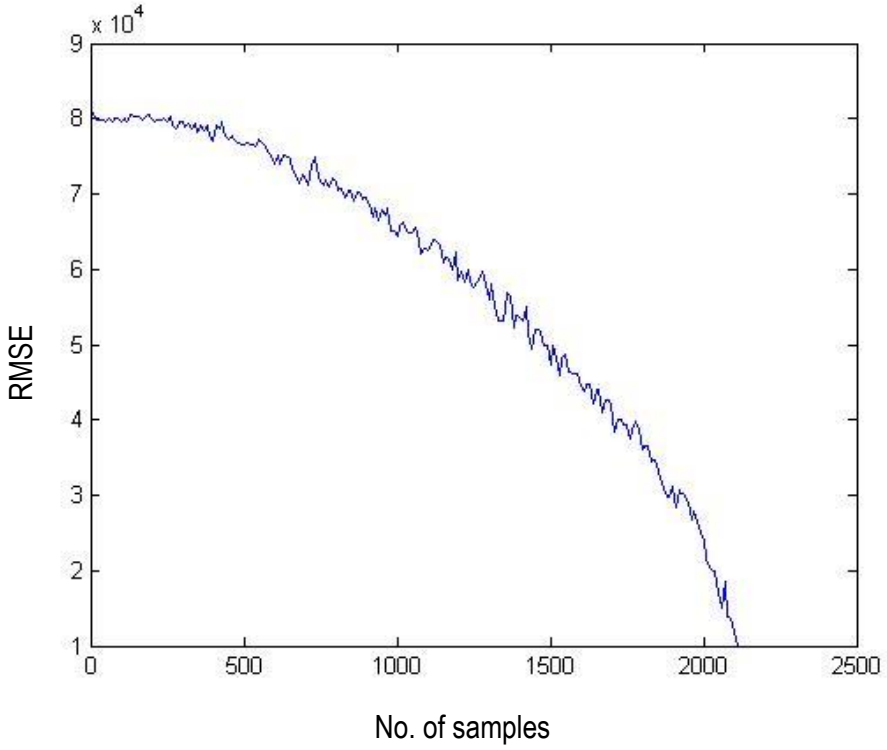


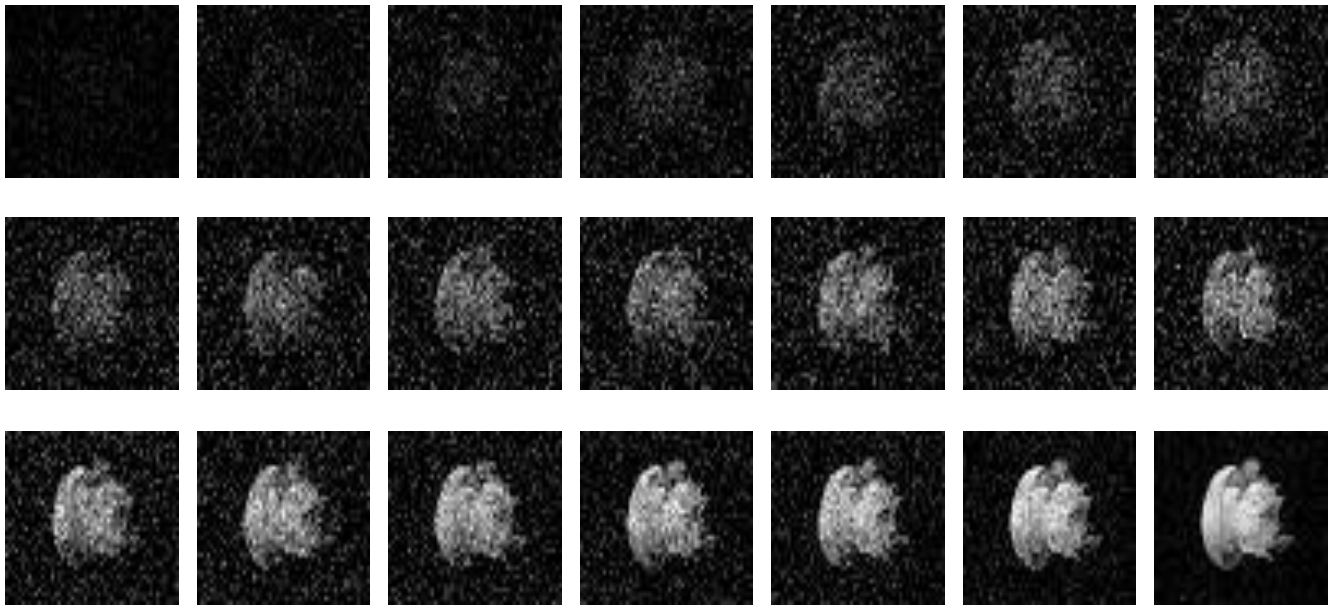
PEDESTRIAN TRACKING

Power efficiency through image representation

- **Feature extraction:** reduction of the dimensionality of visual information by obtaining the most relevant and characteristic points or clusters of points
- **Compressed sensing:** efficient sampling technique that makes use of the sparsity of the signal in some domain

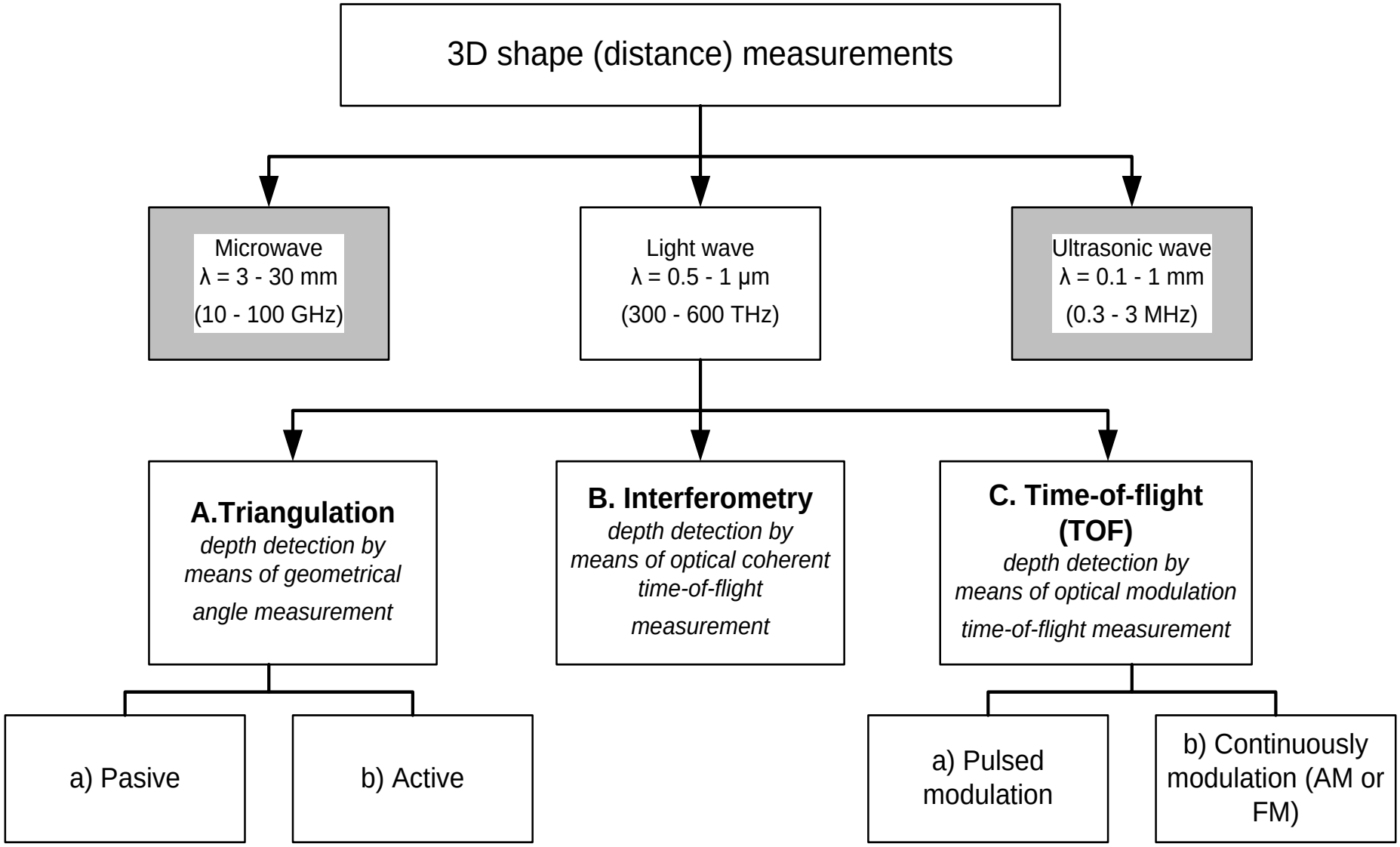
the efficient representation of the scene is conveyed one step further towards the sensors



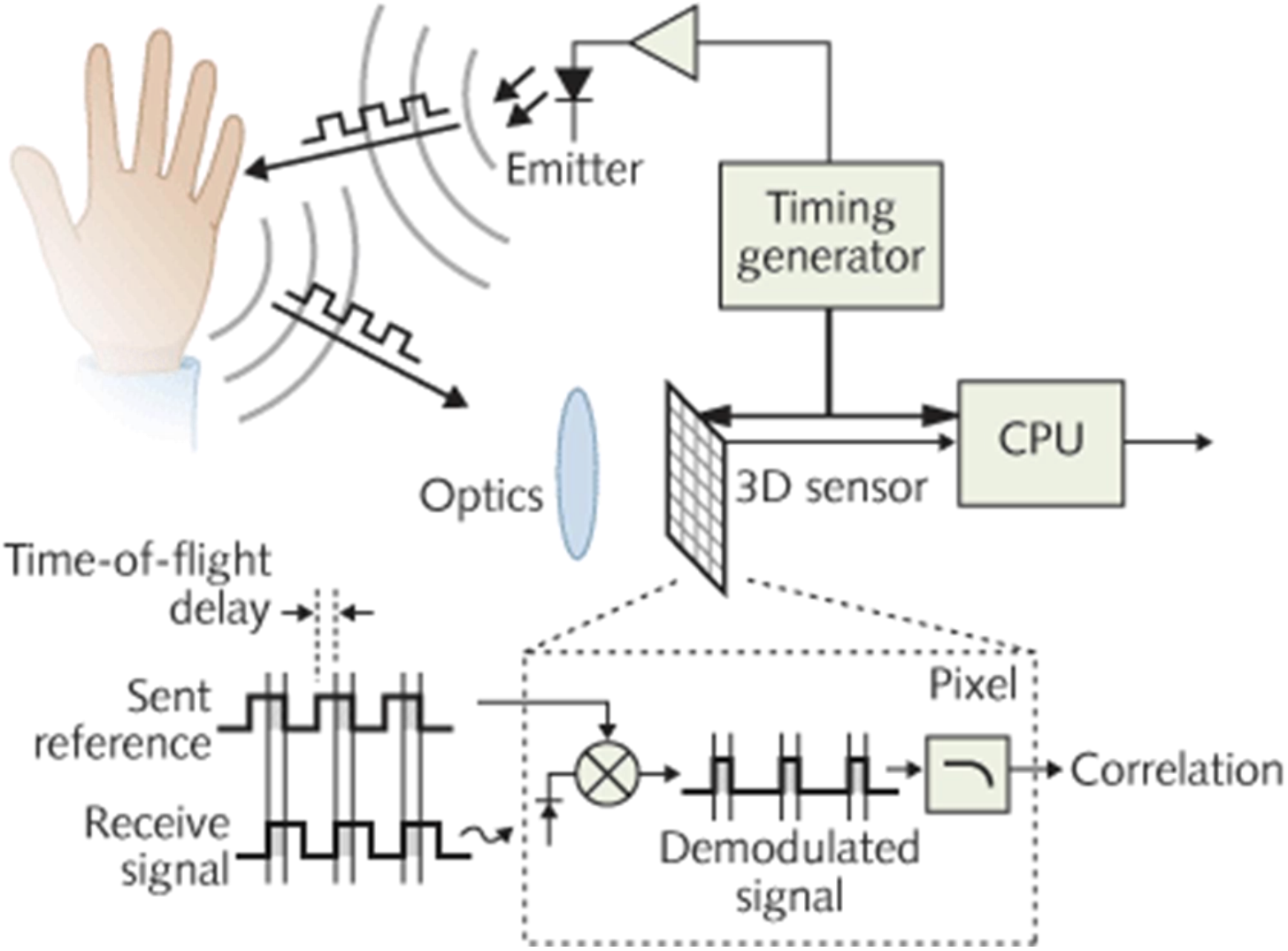


- **Applications:** adaptive image data transmission, high-speed sensing, feature extraction at image sensing, simplification of processing resources at the sensor node

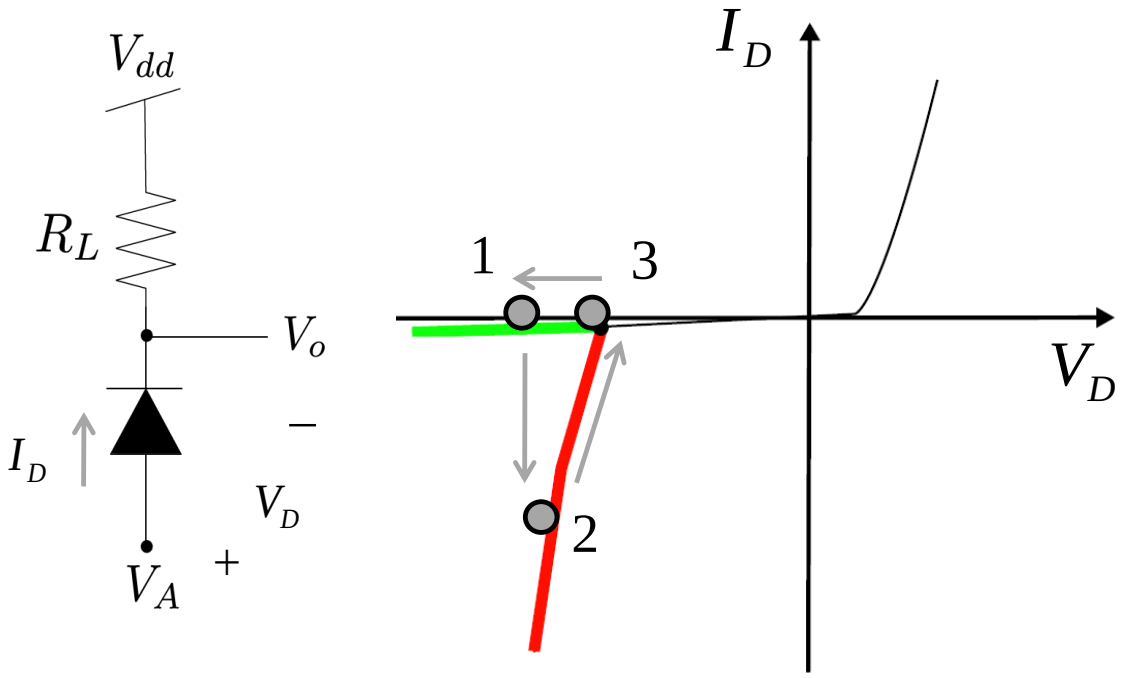
Depth Sensing

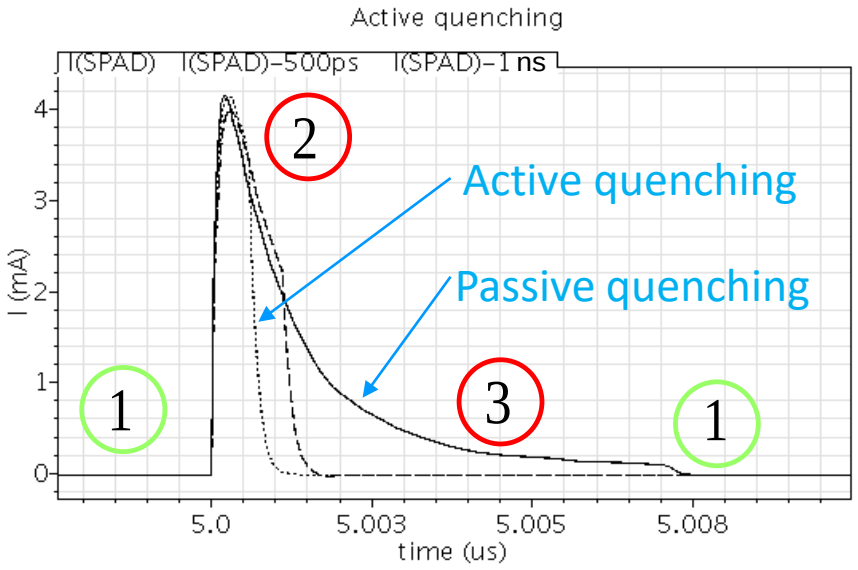


Depth Sensing



Single-photon avalanche photodiodes





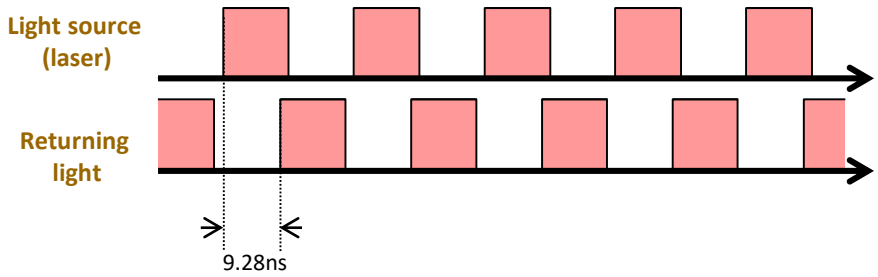
1) A photodiode biased beyond breakdown stays at zero current until avalanche is initiated

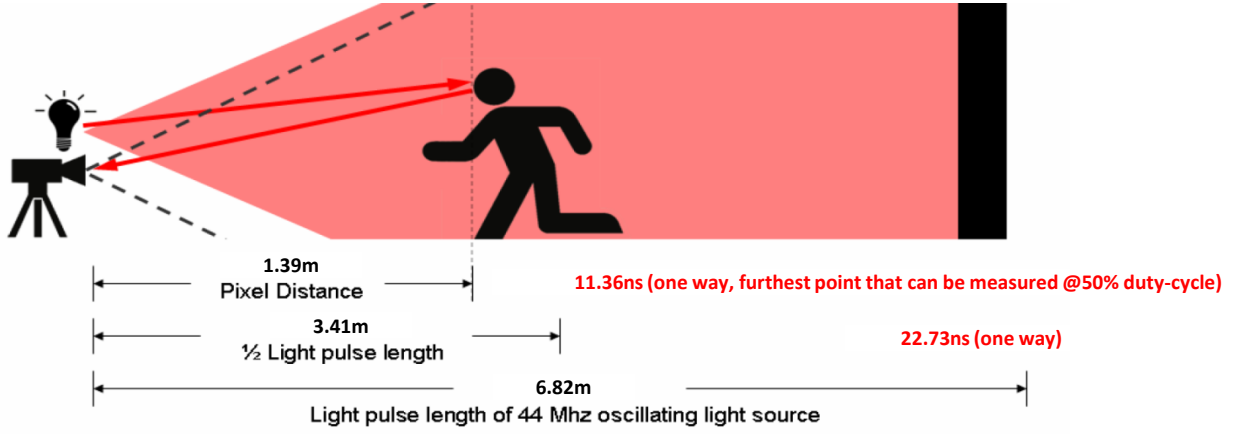
2) Avalanche can be triggered by one single photon absorption event, DC or AP

3) Quenching circuit (active or passive) limits the avalanche current by keeping $|V_0-V_A|<V_{BD}$

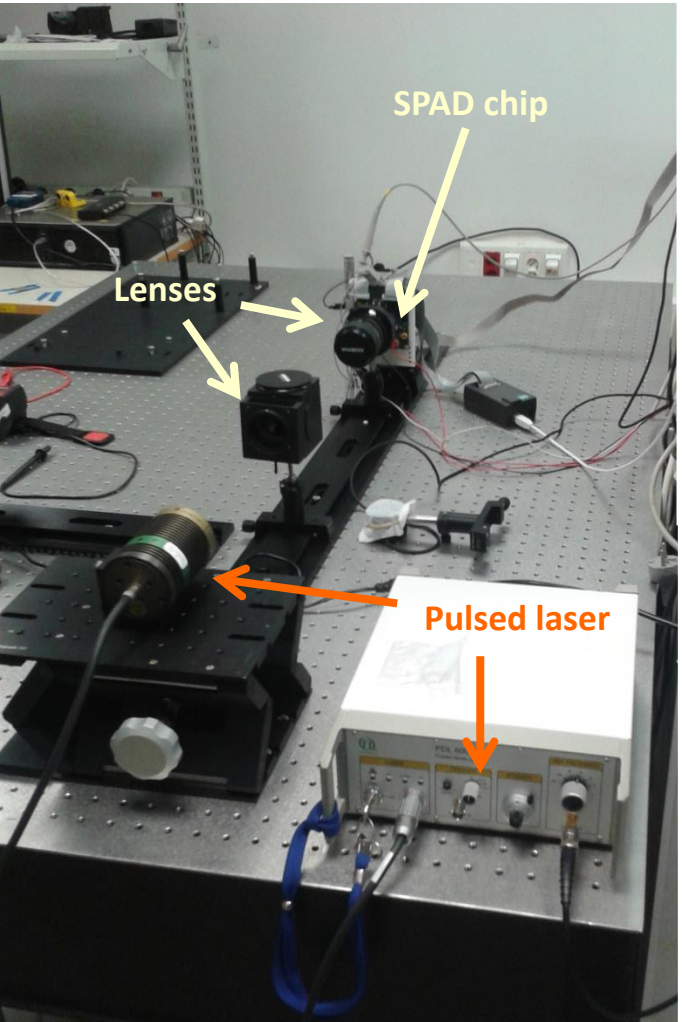
- Avalanche must be quenched to avoid device destruction
- The simplest scheme is passive quenching
- Active quenching and recharge can be employed to decrease dead time

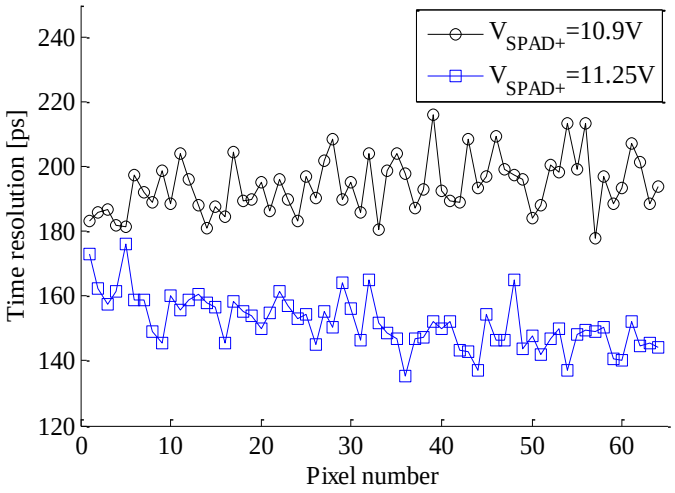
SPAD applications: 3D imaging

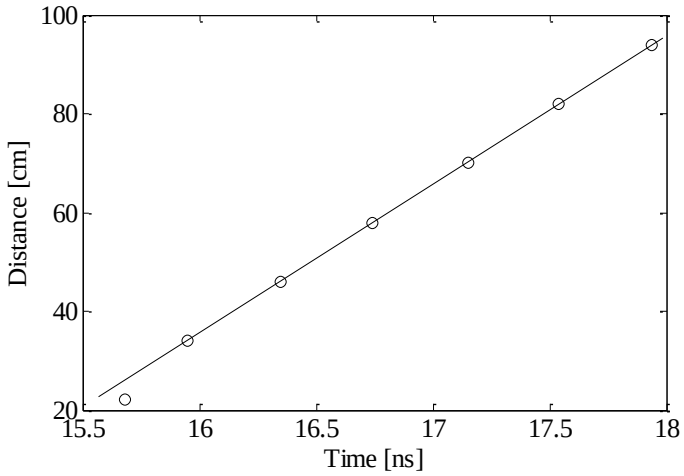


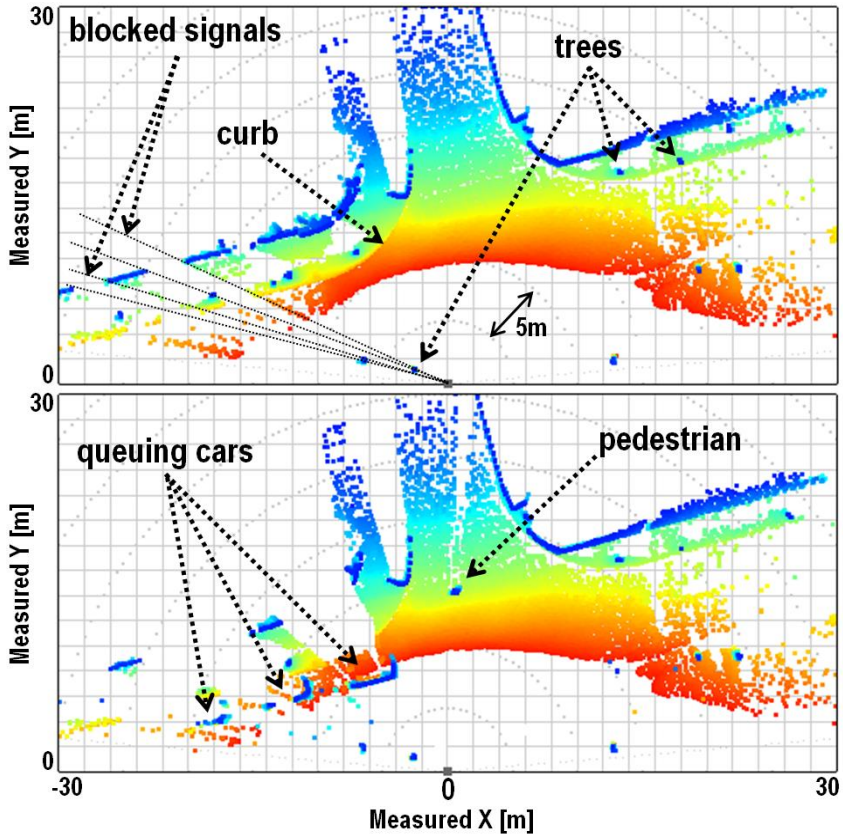


ToF resolution measurement









[Niclass 2011]

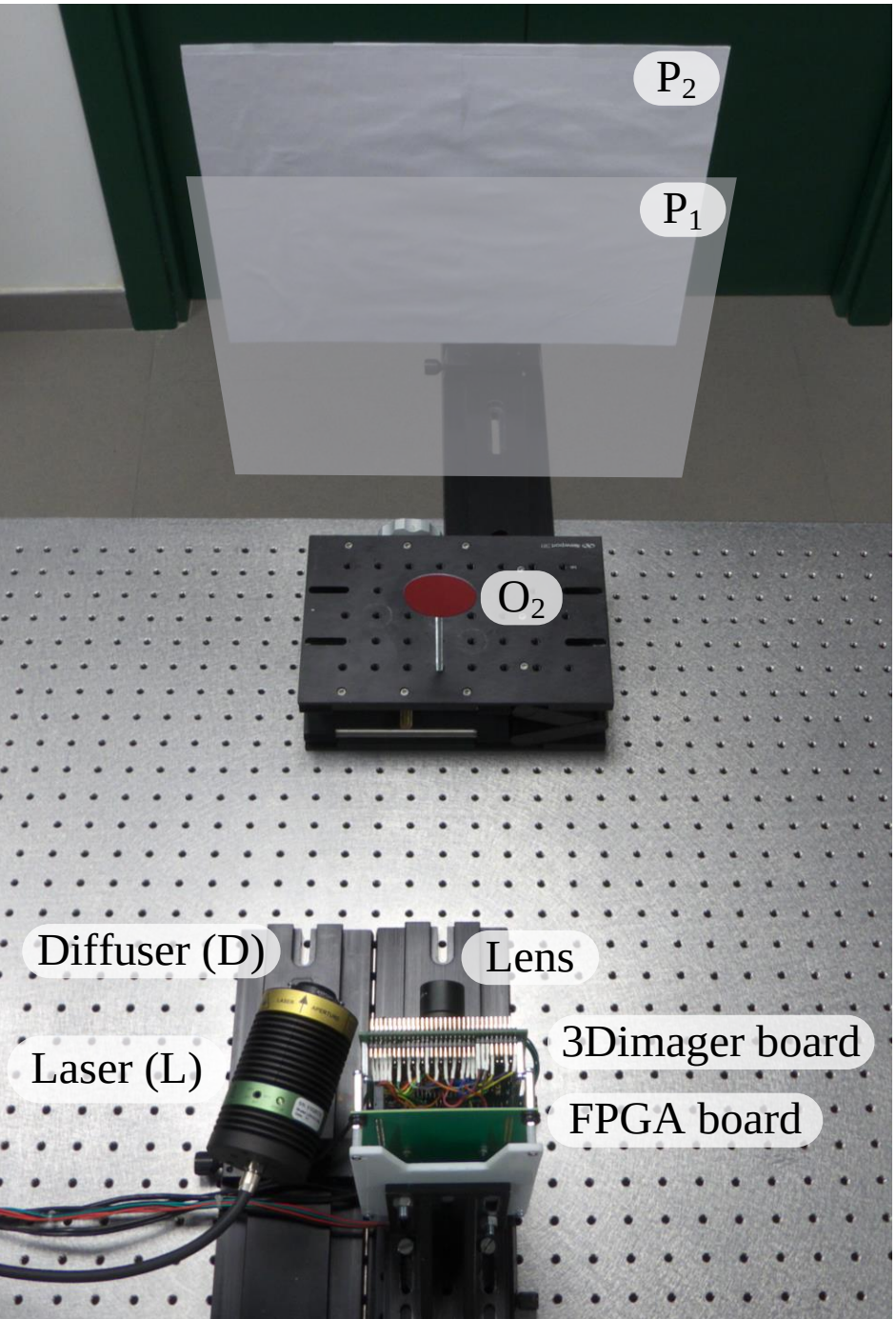
SPAD applications: 3D imaging

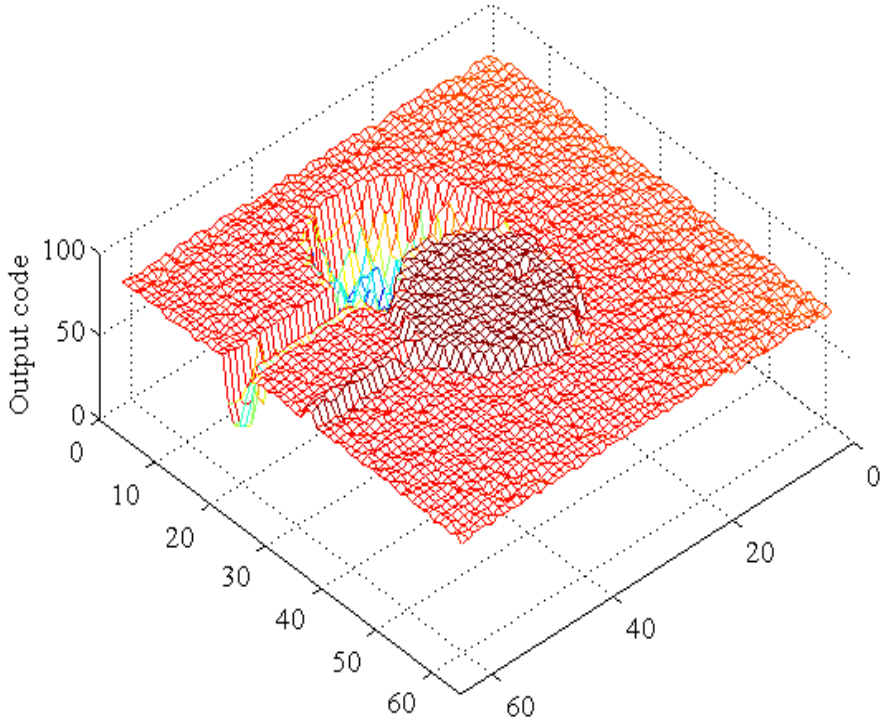
3D Imager with In-Pixel TDC (145ps-ToF)

[Vornicu et al., ISCAS'16]

Best Paper Award of the Sensory Systems Technical Committee

SPAD applications: 3D imaging





SPAD applications: 3D imaging

Performances	[Chuang 2004]	[Gupta 2011]	[Han 2005]	[Vornicu 2016]
Technology	TSMC 0.18µm	TSMC 0.18µm	0.35µm	UMC 0.18µm
Voltage supply	1.8V	3.3V	3.3V	1.8V
Delay cell	Pseudo-differential	Single ended	Differential	Pseudo-differential
Nr. of cells	2	3	4	4
Frequency range	440-1595 MHz (72%)	16MHz-367MHz (95.6%)	1.07 and 2.06 GHz	400-850MHz, (53%)
Nr. of phases	4	3	8	8
K_{VCO}	Non-linear	153MHz/V	561MHz/V	477MHz/V
Linearity	87.3%	68.6%	-	99.4%
Phase noise [dBc/Hz]	-93 @1MHz	-88 @100KHz	-99 @2MHz	-102 @2MHz
Area/A_{VCRO}	3.11	1.53	-	1
Avg. power	26mW	35.5mW	14.6mW	1.17mW