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University of Cagliari

**AUTOMATIC GENERATION OF
DATAFLOW-BASED LOW-POWER
RECONFIGURABLE SYSTEMS**

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CPS DESIGN
FROM CONCEPT TO IMPLEMENTATION

Cyber Physical Systems

CGR approach for high run-time adaptivity

Complex systems with different **interacting components**, that need to **adapt** their behavioural modality according to **functional** and **non-functional** requirements.



<http://www.cerberus-h2020.eu/>



Cyber Physical Systems

CGR approach for high run-time adaptivity

Complex systems with different **interacting components**, that need to **adapt** their behavioural modality according to **functional** and **non-functional** requirements.

Adopting **Coarse Grain Reconfigurable Approach** to achieve high run-time adaptivity.



<http://www.cerberus-h2020.eu/>



MULTI DATAFLOW COMPOSER TOOL

Coarse-Graine Reconfiguration

**Multi Dataflow
Composer Tool**

Structural Profiler

Power Manager

*Co-Processor
Generator*

MDC design suite

<http://sites.unica.it/rpct/>

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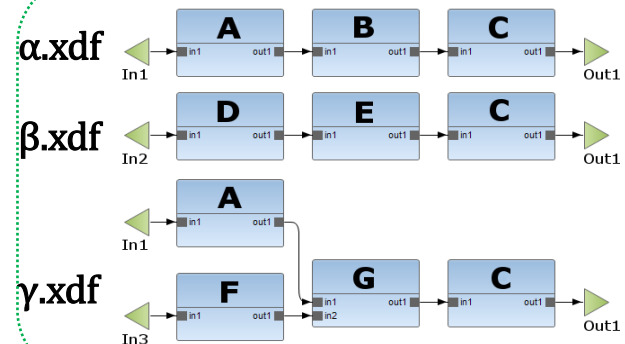
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Dataflow Specifications



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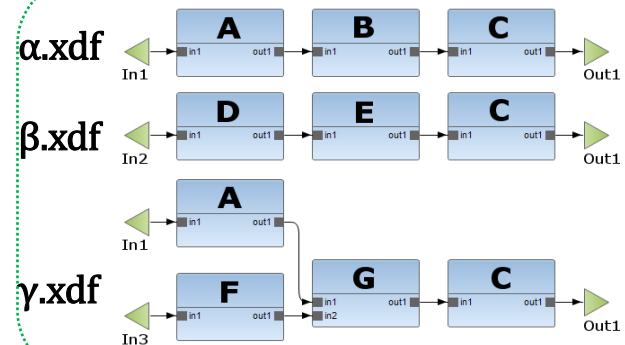
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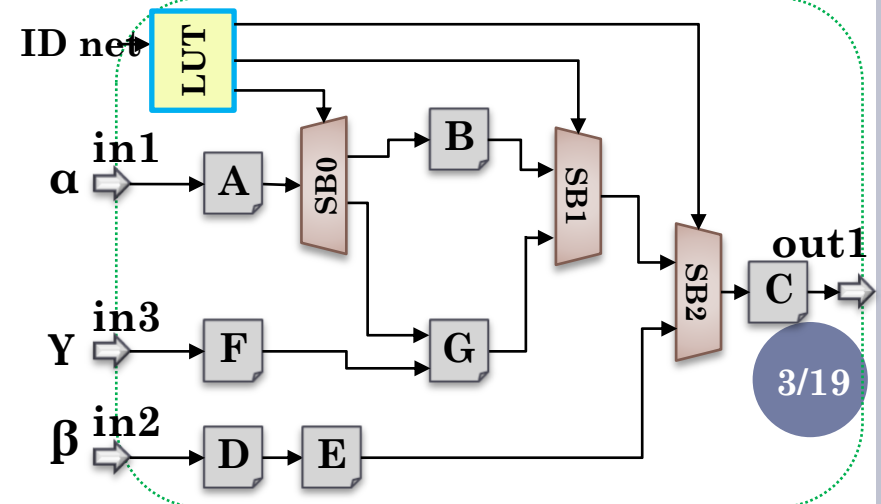
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Dataflow Specifications



N:1

Coarse Grained Reconfigurable Platform



MULTI DATAFLOW COMPOSER TOOL

Additional features

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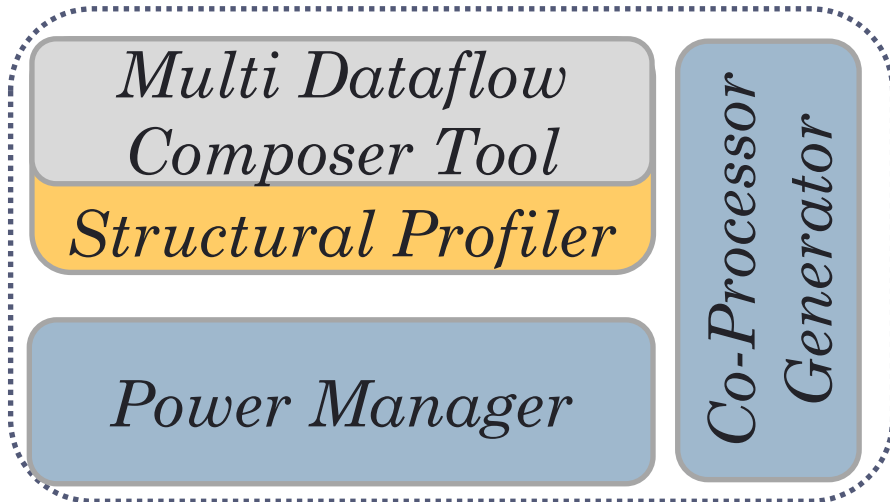
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Additional features



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Structural Profiler:

low-level feedback (from synthesis) and DSE for topology optimization.

- (ASIC + FPGA)

Co-Processor Generator:

generation of ready-to-use Xilinx Ips

- (FPGA)

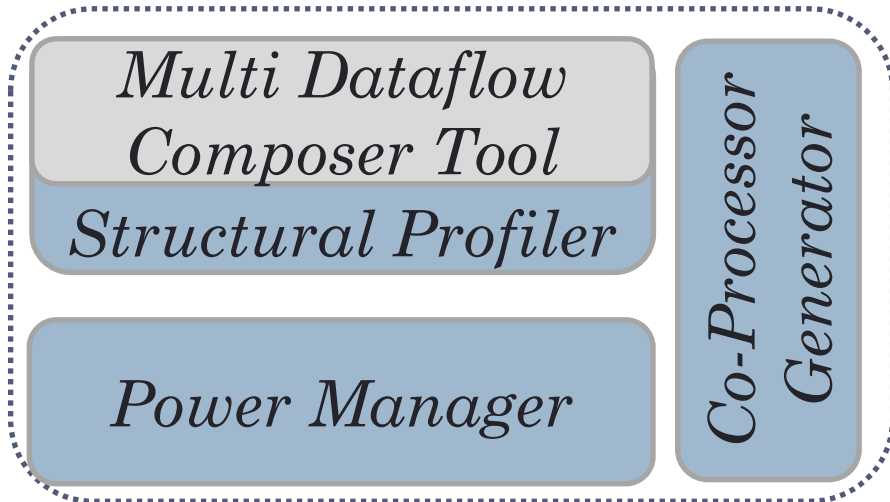
Power Manager:

automatic application of clock-gating and/or power-gating.

- CG (ASIC + FPGA)
- PG(ASIC)

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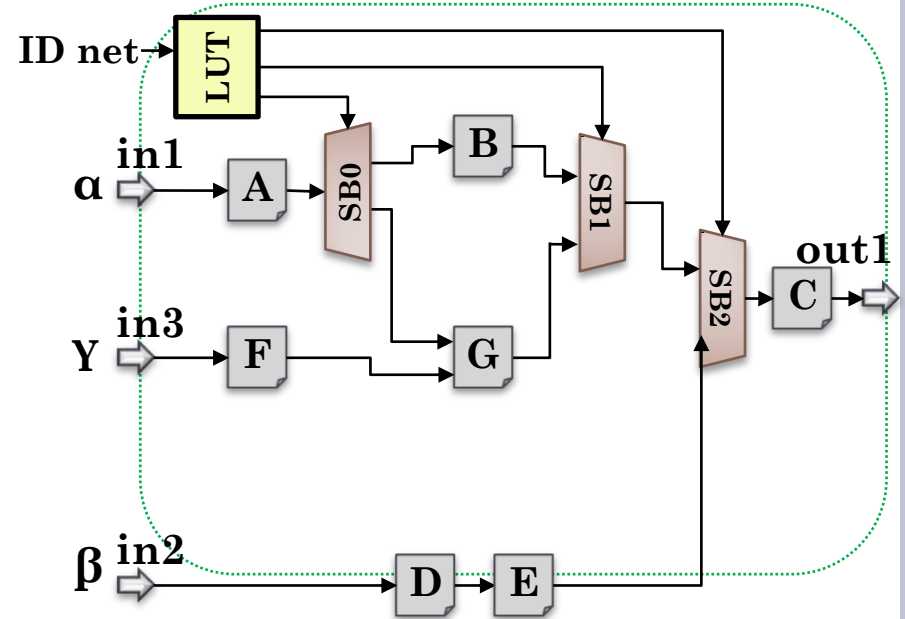
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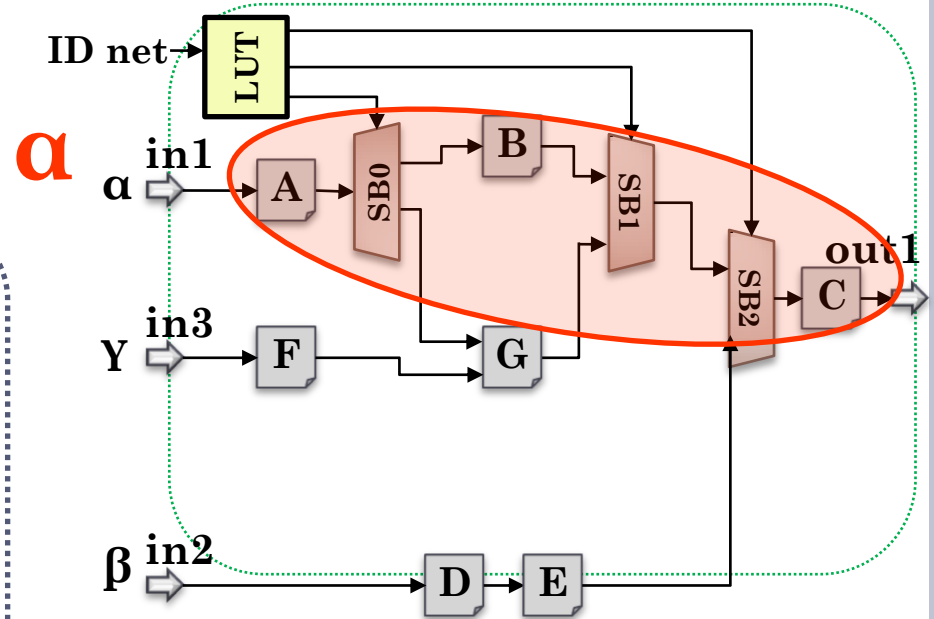
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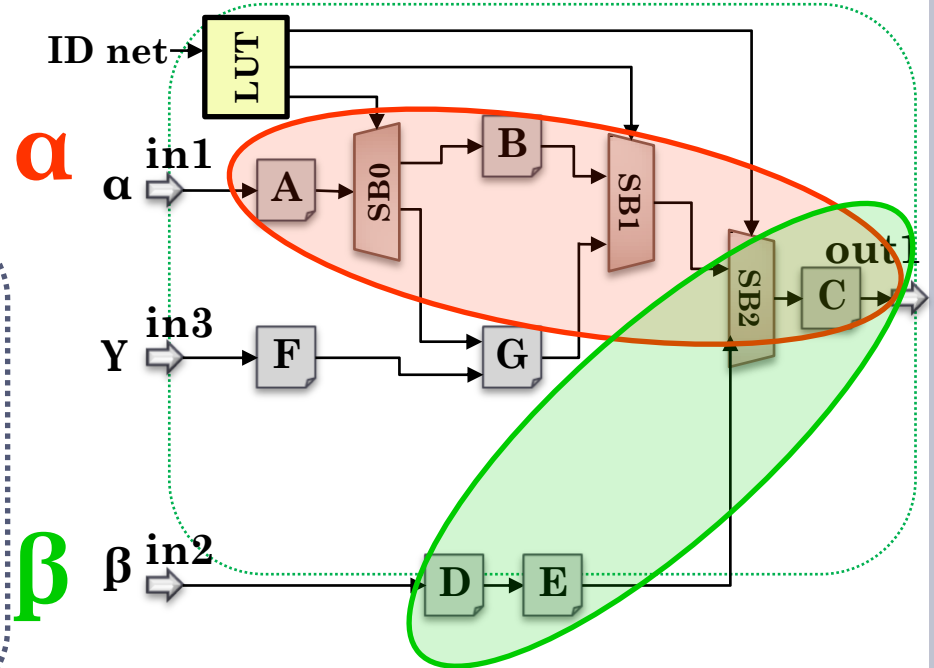
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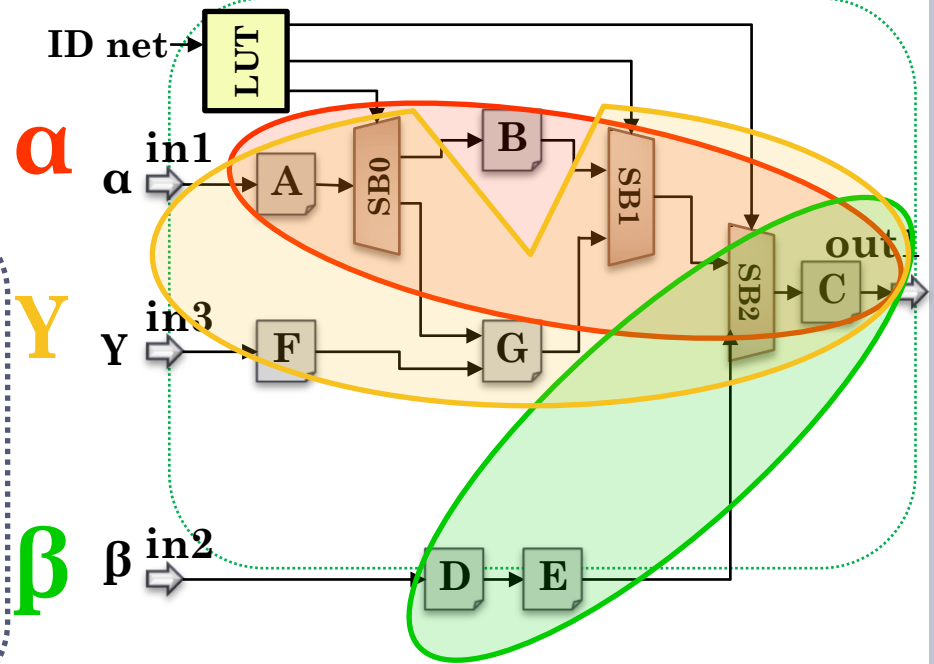
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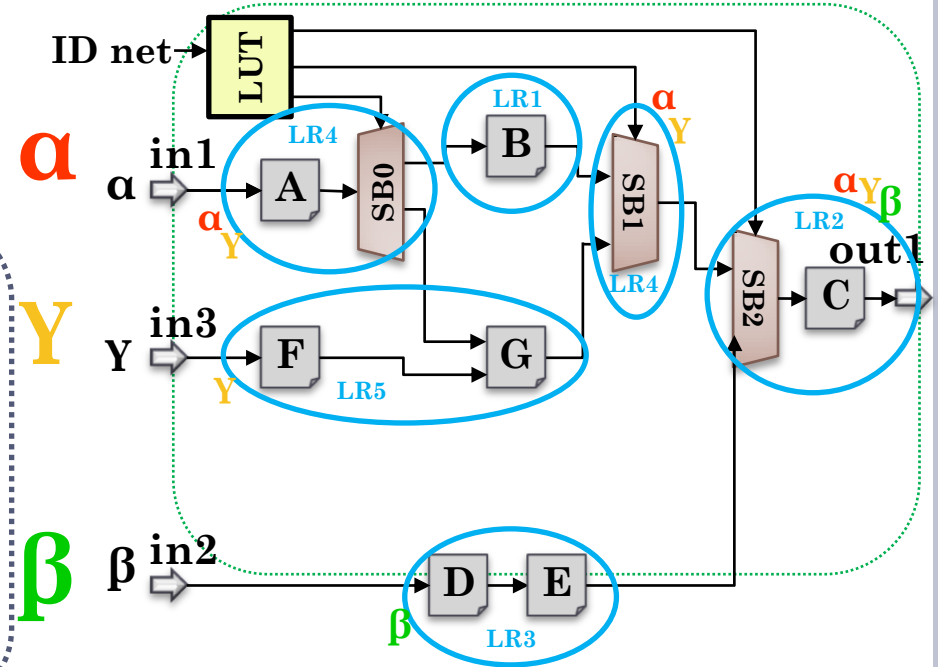
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Acknowledgements

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