

HW/SW Cyber-System Modeling Tools

**Julio
OLIVEIRA**

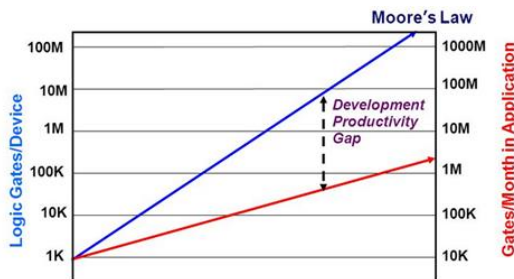
**Karol
DESNOS**

HW/SW Cyber-System Modeling Tools

1. Modeling Environment and Languages
2. (HW &) SW Synthesis
3. Simulators
4. Verification / Validation
5. Runtime Support

From System Models to Value

The topic of this lecture



Communicate

Validate - Verify

Configure

Analyze

Simulate

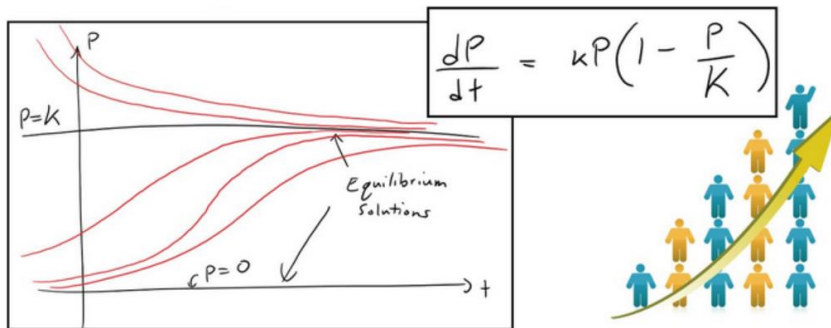
Decide

Optimize

Automation !

A short recap from CPS Modeling lecture

We talked about models ...



... and about modeling for CPS.



**Abstraction
(Simplification)**

**Description
(Specification)**

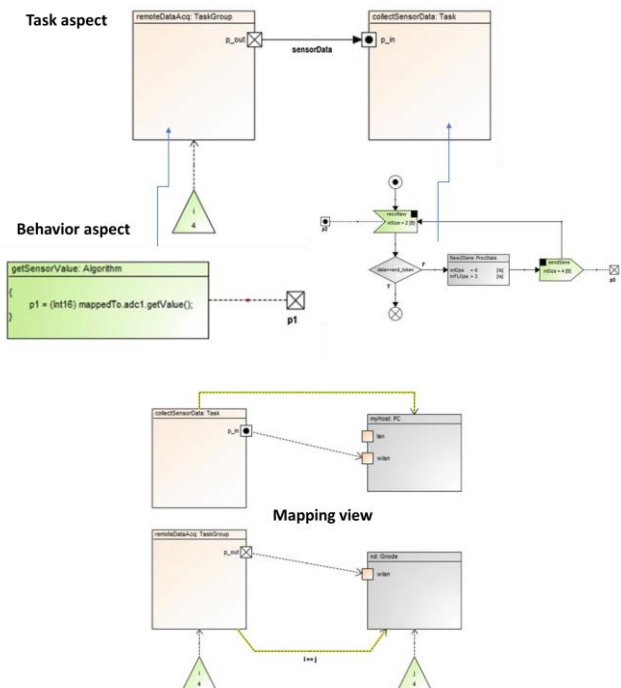
**Operational
(Executable)**

A short recap from CPS Modeling lecture

We talked about multi-aspect modeling...

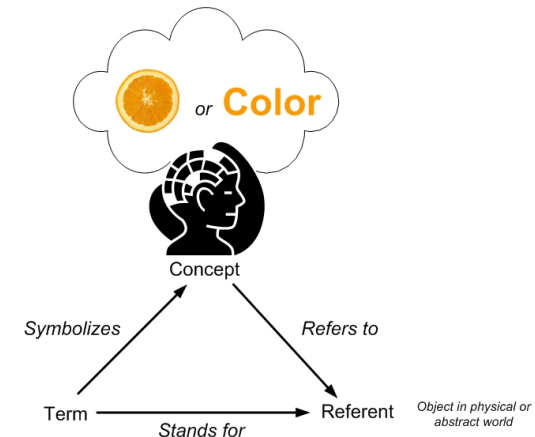
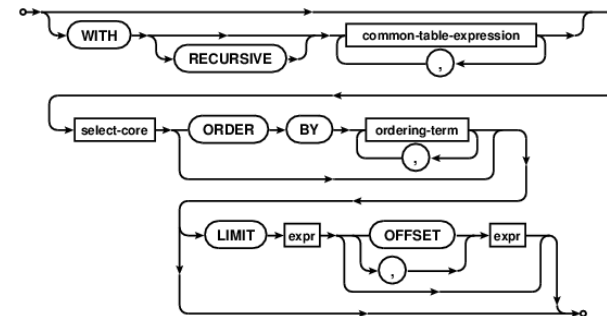
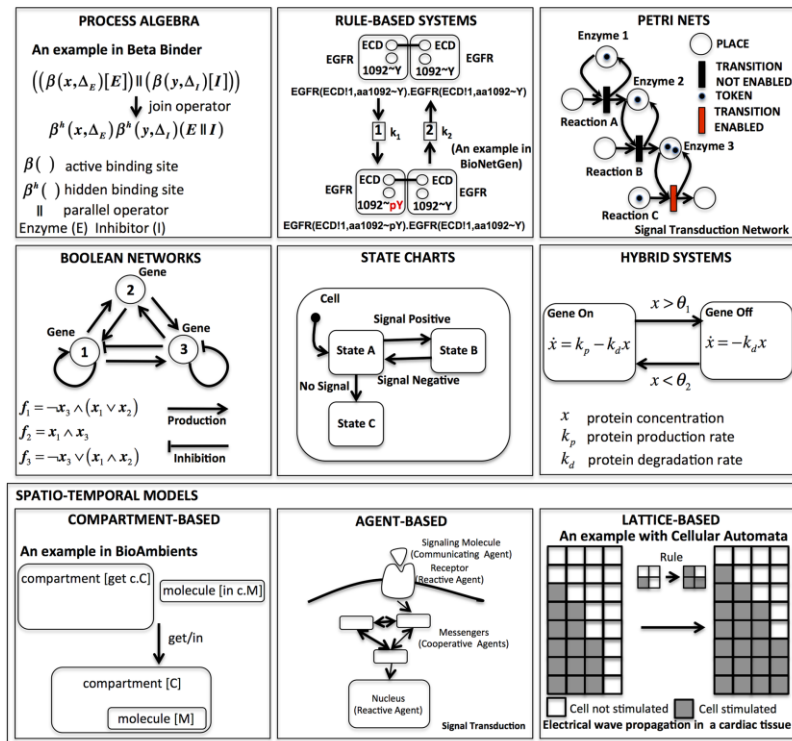


... and illustrated how aspects can be combined to extract KPIs.



Last, but not least...

We went into details about Semantics, Syntax, Models of Computation and Models of Architecture

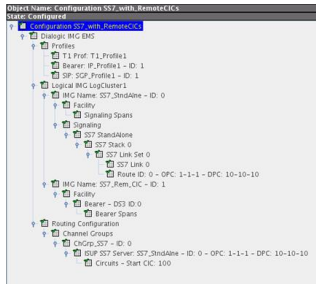


“Orange”

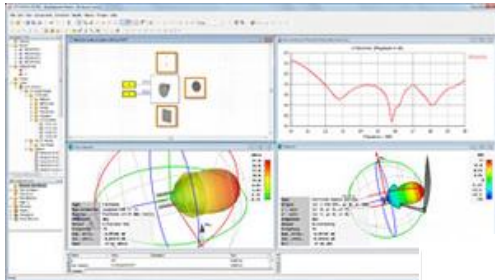


Making more of a model

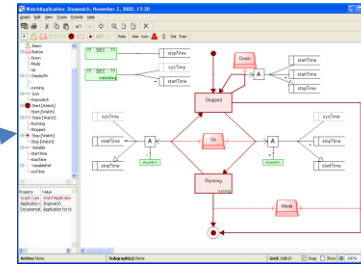
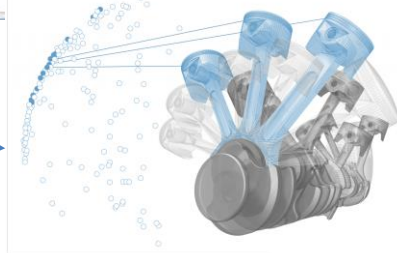
Configuration



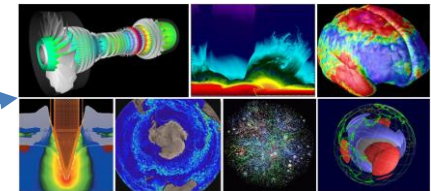
**Analysis
Validation / Verification
Simulation**



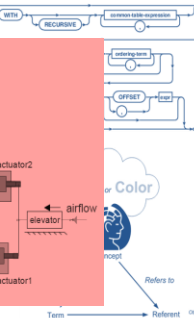
**Automatic design
Design space exploration
Decision making**



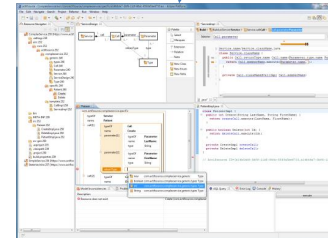
**Modeling
environment**



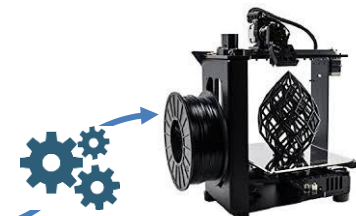
**Visualization
Presentation**



Term Stands for
"Orange" or Color



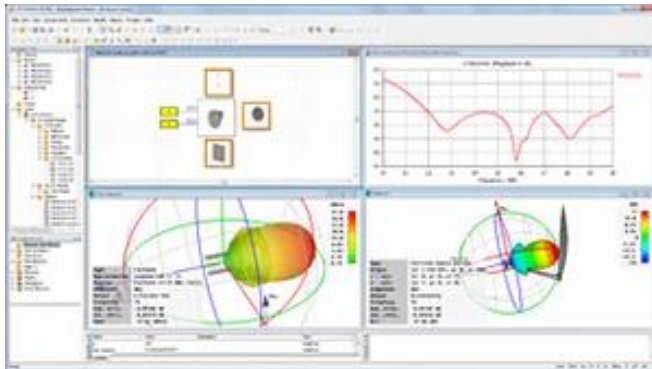
Code synthesis



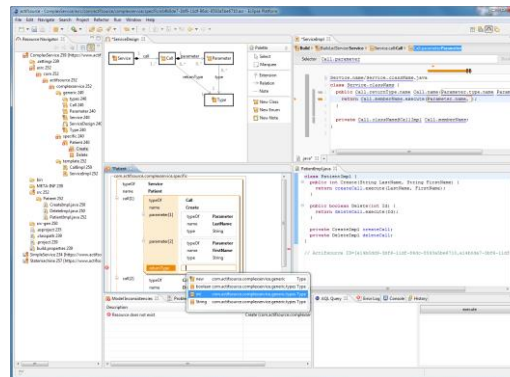
Implementation

In this lecture

Analysis
Validation / Verification
Simulation



Code synthesis



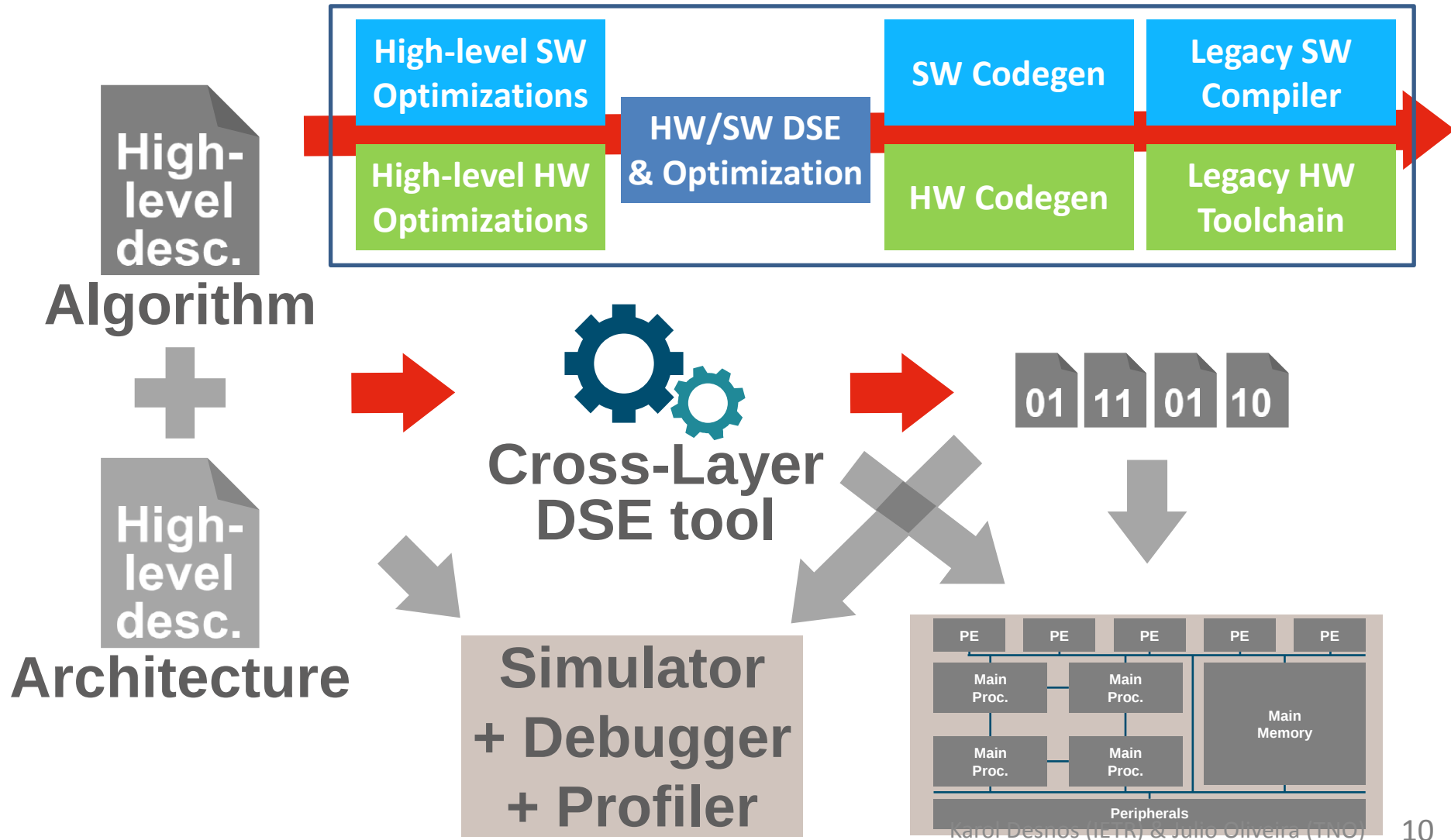
Compilers for adaptive systems



HW/SW Cyber-System Modeling Tools

1. Modeling Environment and Languages
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3. Simulators
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5. Runtime Support

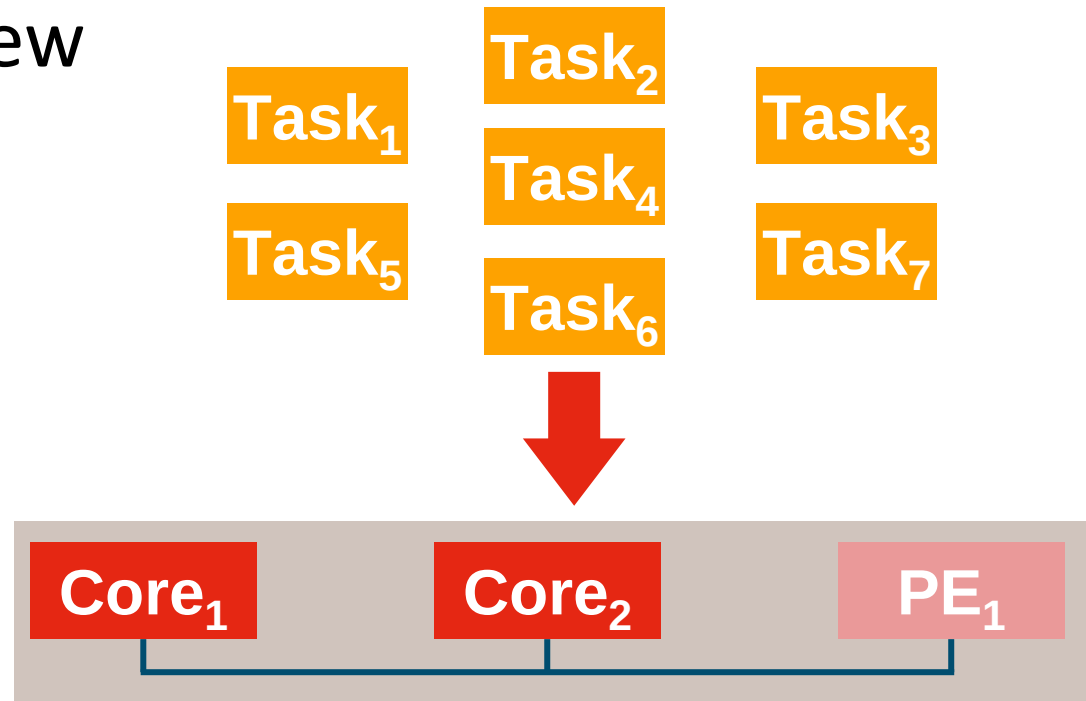
Synthesis at component level?



SW synthesis > overview

Task Management

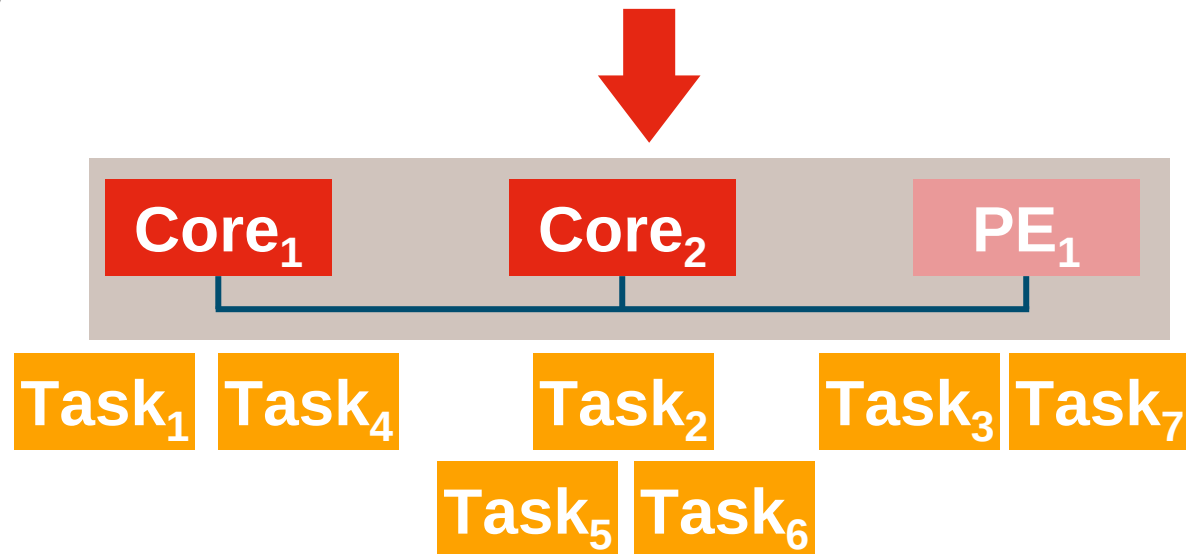
- Assignment (Mapping)
- Ordering (Scheduling)
- Timing



SW synthesis > overview

Task Management

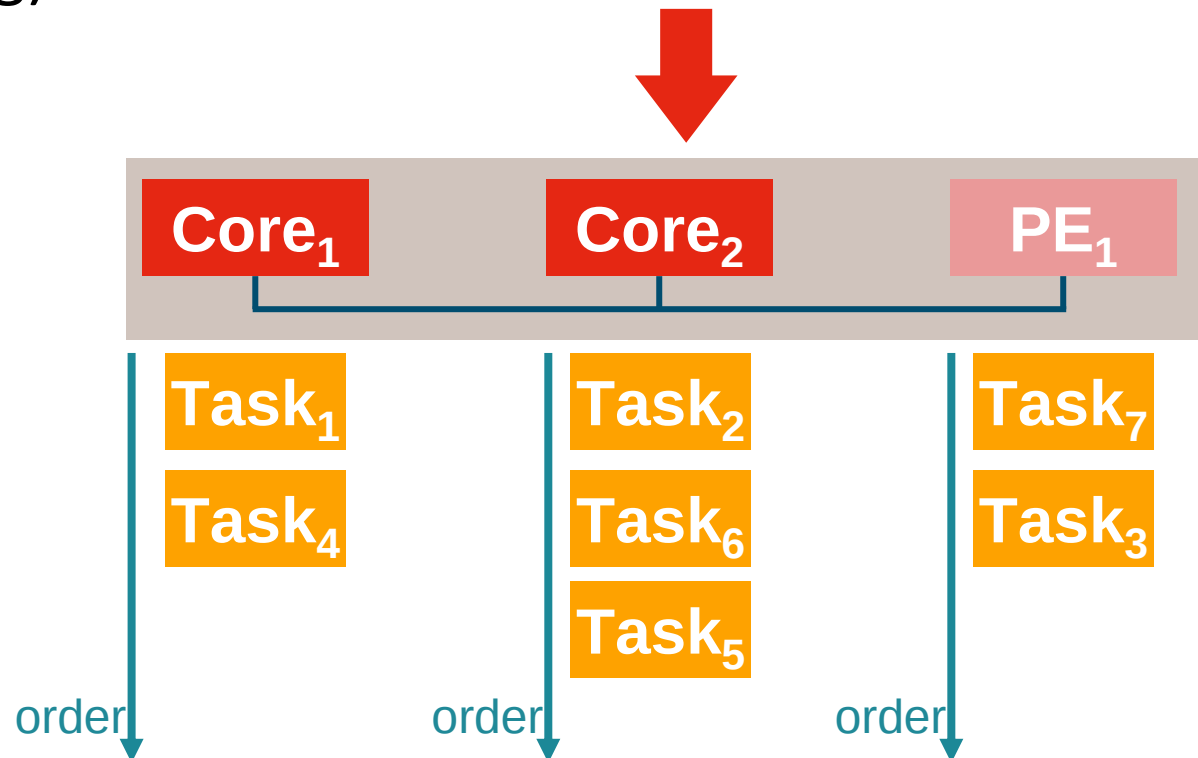
- Assignment (Mapping)
- Ordering (Scheduling)
- Timing



SW synthesis > overview

Task Management

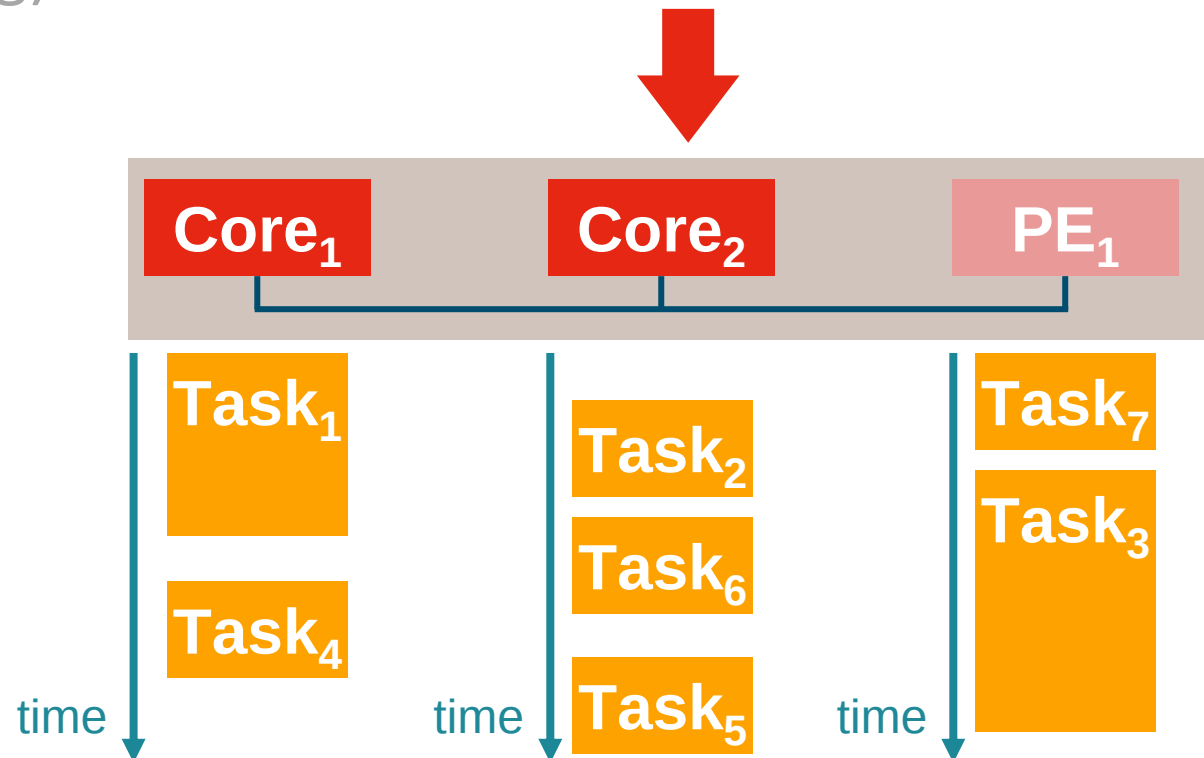
- Assignment (Mapping)
- Ordering (Scheduling)
- Timing



SW synthesis > overview

Task Management

- Assignment (Mapping)
- Ordering (Scheduling)
- Timing



SW synthesis > HW management

Task Management

- Assignment (Mapping)
- Ordering (Scheduling)
- Timing

Communication

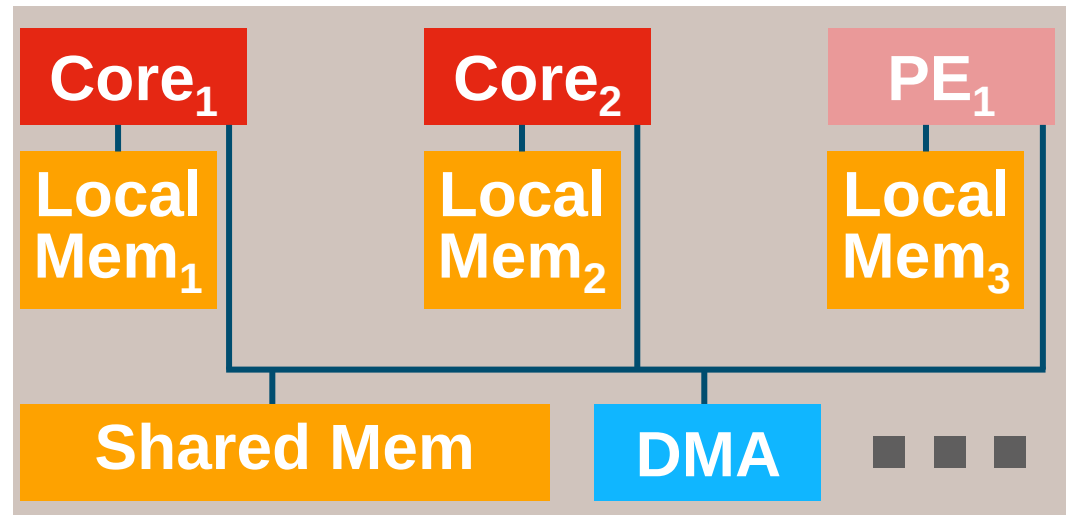
- Direct copy
- DMA
- Ordering

Synchronization

- Polling
- Interrupts

Memory

- Static Allocation
- Dynamic Allocation
- Model-based allocation



SW synthesis > Complexity

HW resources heterogeneity

- Processing Elements / Interconnect / Memory

Limited HW resources

- PE / Interconnect / Memory

SW model complexity

- Complex control dependency
- Complex data dependency
- Low predictability

SW synthesis > Tools & methods objectives

Optimizing / offering trade-offs between:

- Latency / Response time
- Throughput
- Load balancing
- Memory footprint
- Power consumption

Adaptability to any target architecture:

- DSP
- GPU
- HPC

Mapping/Scheduling > Problem

Part of “Operational Research”

- How to organize a production line, train schedule, ...
- How to organize a project (Gantt Chart, ...)
- How to make decisions in general

NP-Complete Problem

- **Validity of a solution** to the problem can be **verified in polynomial time** (e.g. verifying that a schedule is valid).
- **No polynomial time algorithm** for solving NP-complete problems is known (and it is likely that none exists).
- When the **problem grows** (e.g. number of cores or tasks), solving it is becoming **more complex exponentially**.

Mapping/Scheduling > Solutions

Heuristic algorithms

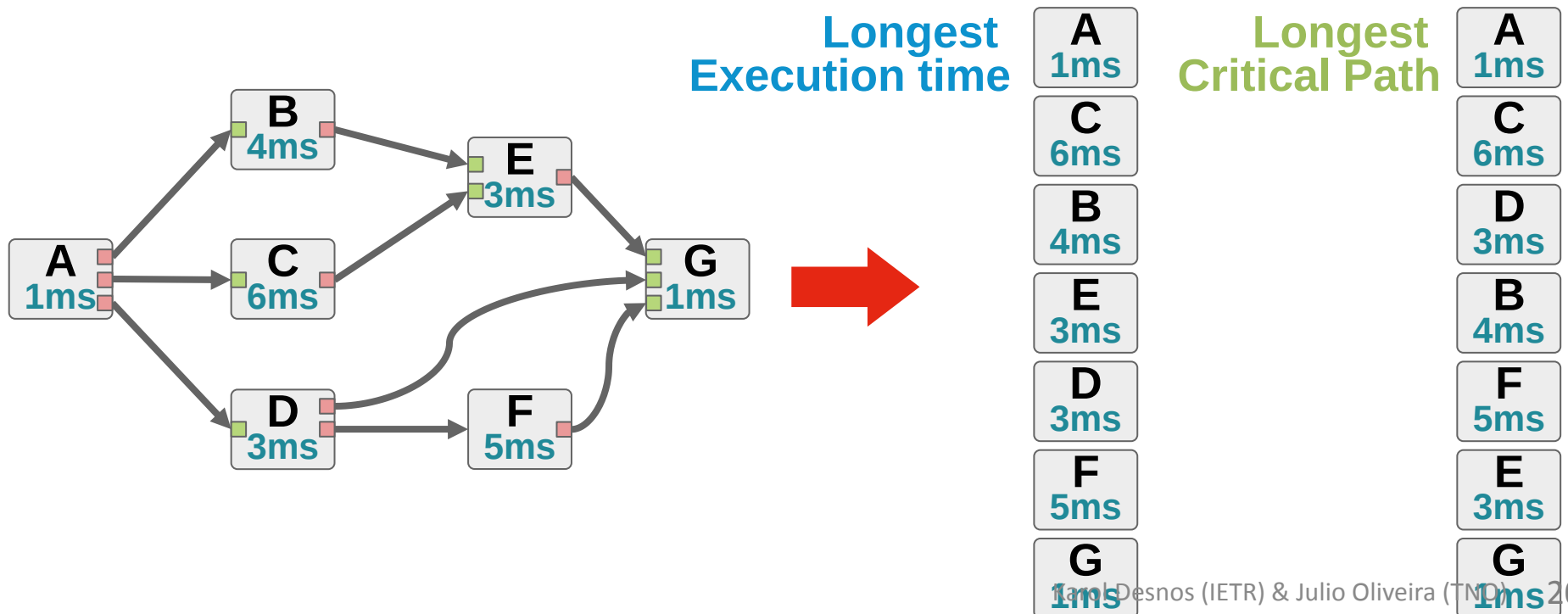
- Find a sub-optimal solution in polynomial time
- No guarantee on the solution quality

	Problem Specific	Generic Algorithms
Constructive	• List scheduling • Greedy scheduling • Hybrid flow-shop	• Divide and conquer • Branch and bound
Iterative	• FAST scheduling	• Integer Linear Programming • Genetic Algorithms • Simulated annealing • Ant colony

Mapping/Scheduling > List scheduling for dataflow

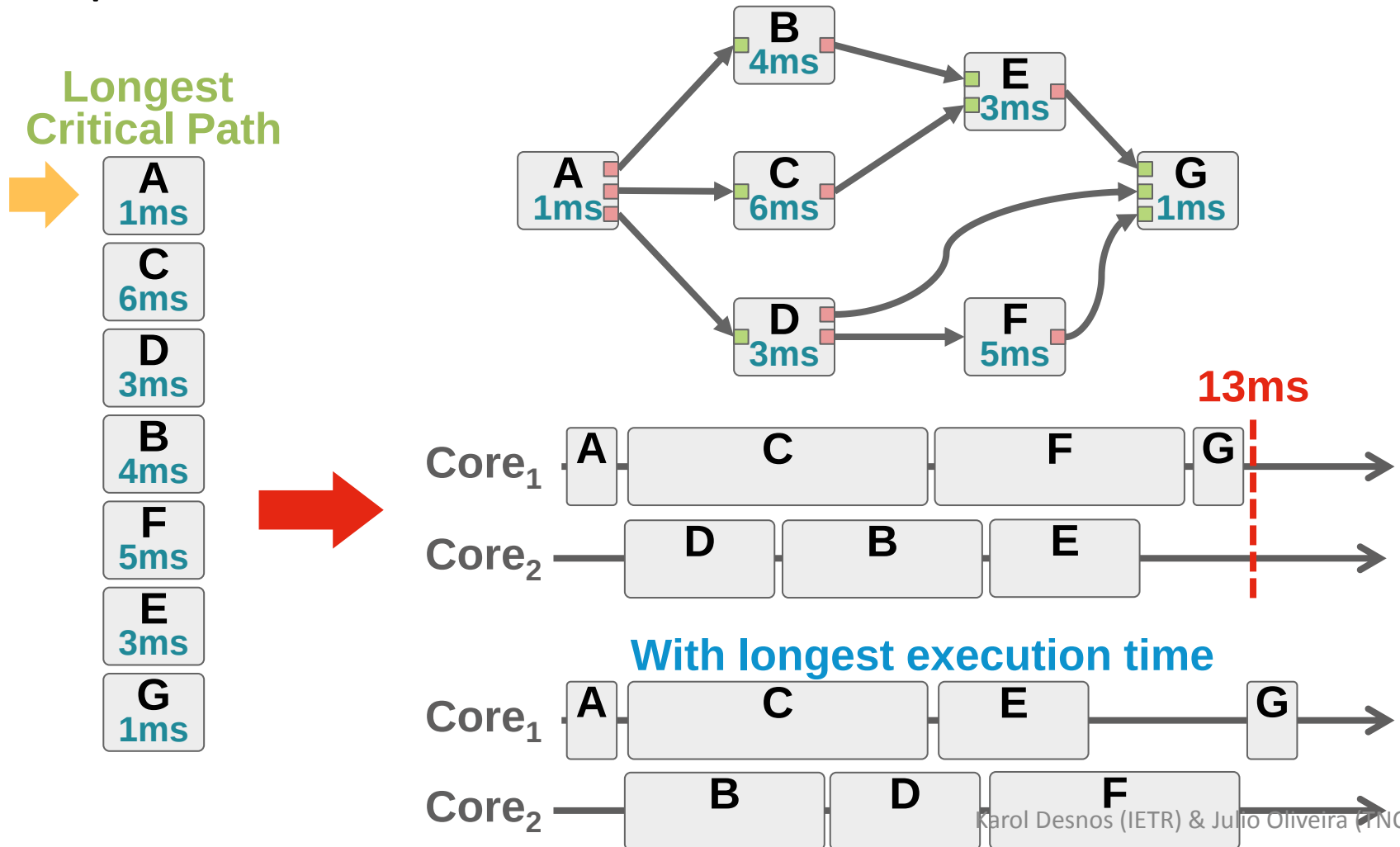
1. Create a list of actors sorted in:

- Topological order (i.e. data dependency order)
- When equivalent, secondary sorting criteria is used:
longest execution time, critical path before last task, ...



Mapping/Scheduling > List scheduling for dataflow

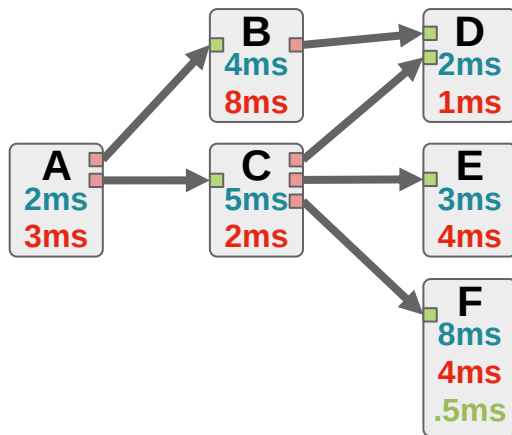
2. Map and schedule actors to the first available PE:



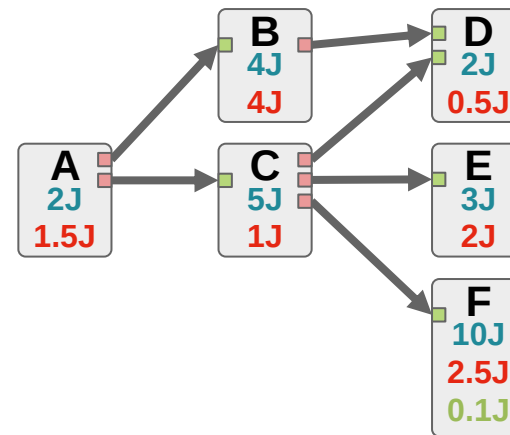
Mapping/Scheduling > Multi-objective optimization

E.g. Latency and power on heterogeneous target.

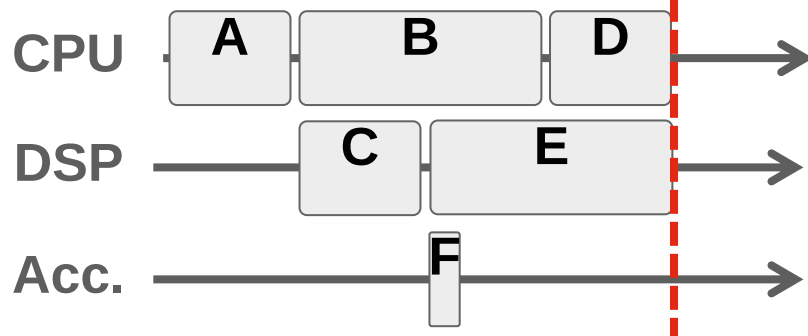
Time



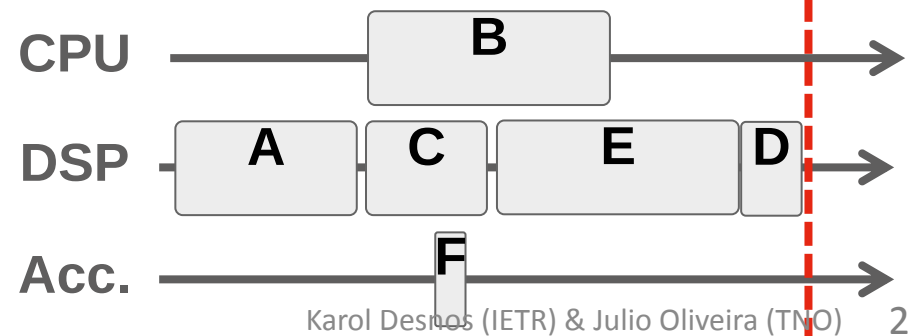
Power



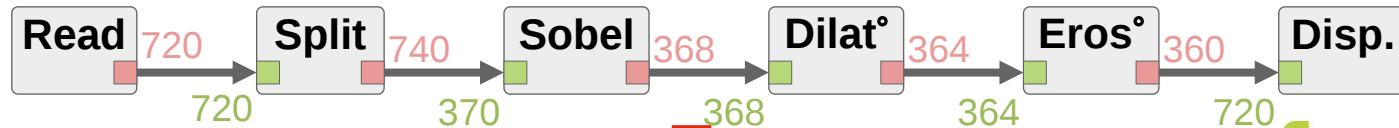
8ms – 11.1J



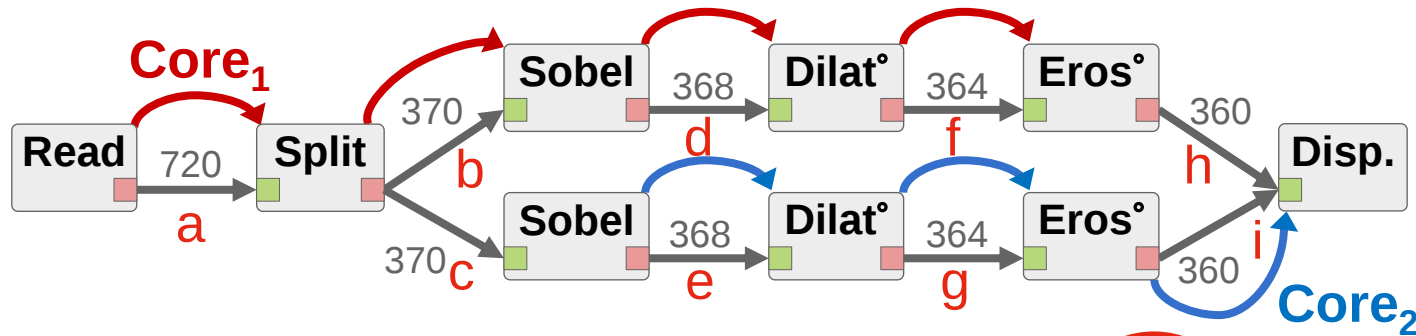
10ms – 9.1J



Memory Allocation



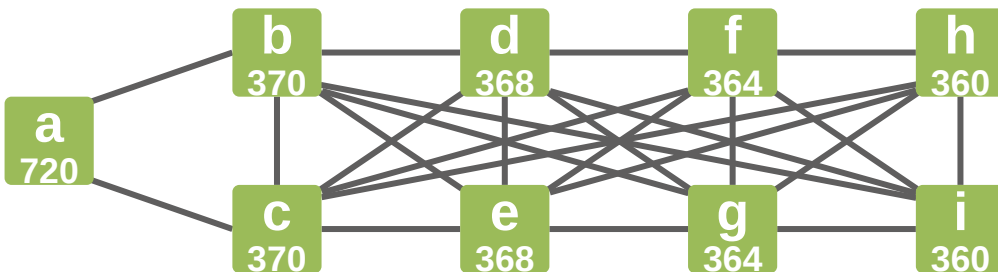
1 Transform



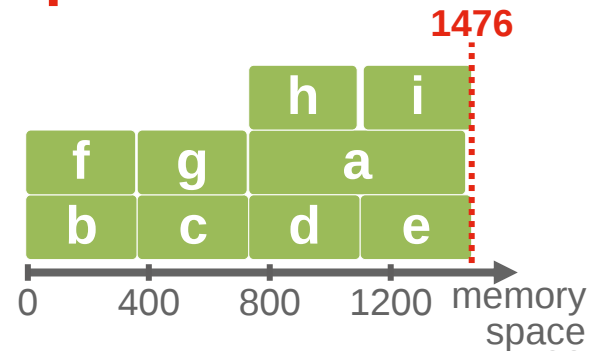
2 Model

3 Update

4 Allocate



Memory Exclusion Graph (MEG)



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- 3. Simulators**
4. Verification / Validation
5. Runtime Support

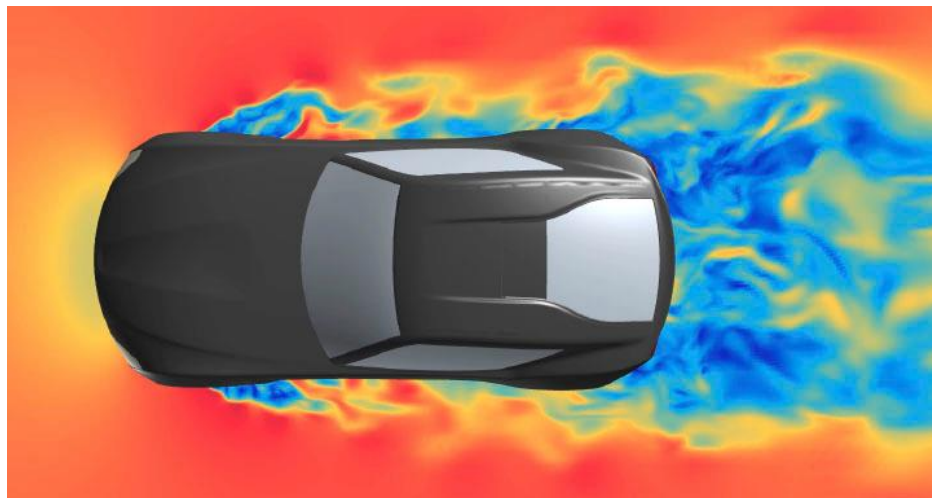
Simulation

From Wikipedia, the free encyclopedia

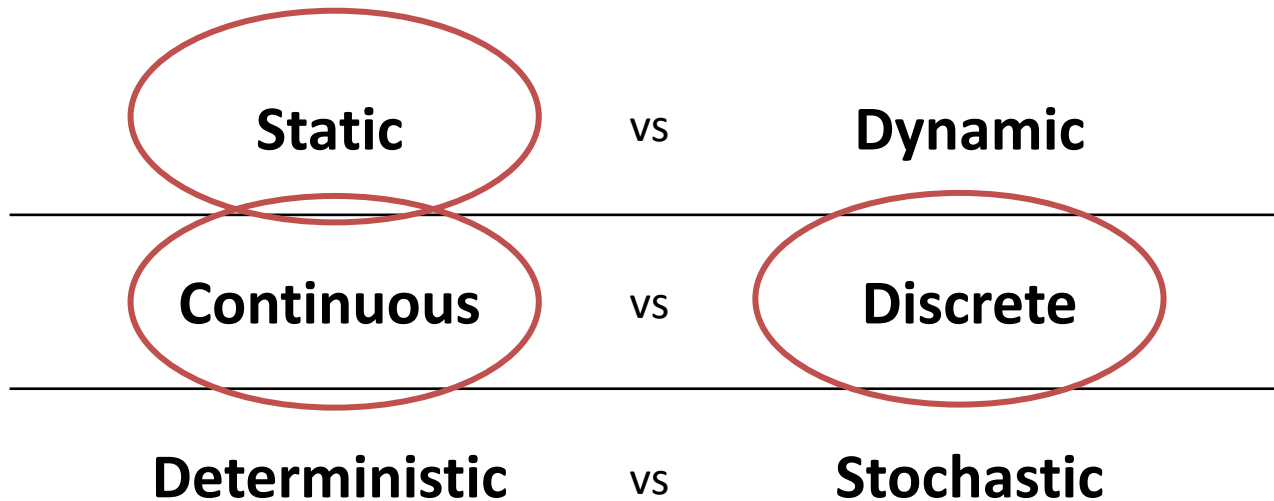
Not to be confused with [Stimulation](#).

"[Simulator](#)" redirects here. For other uses, see [Simulator \(disambiguation\)](#).

Simulation is the [imitation](#) of the operation of a real-world process or system over [time](#).^[1] The act of simulating something first requires that a model be developed; this model represents the key characteristics, behaviors and [functions](#) of the selected physical or abstract system or process. The model represents the system itself, whereas the simulation represents the operation of the system over time.



Types of simulators

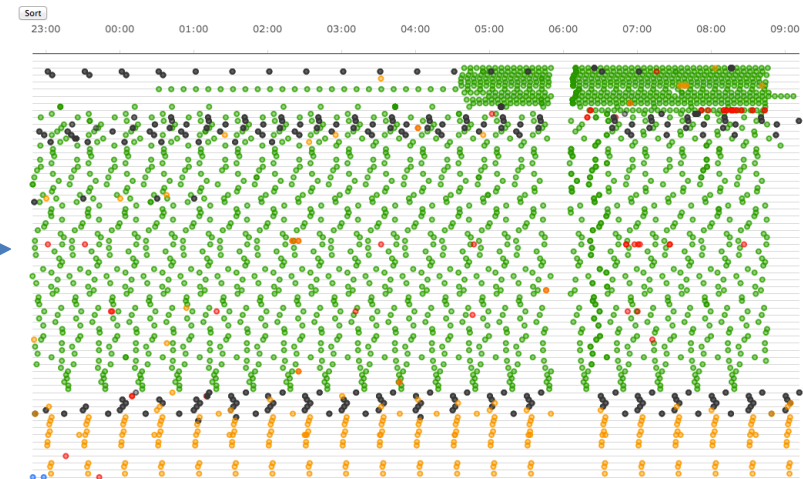
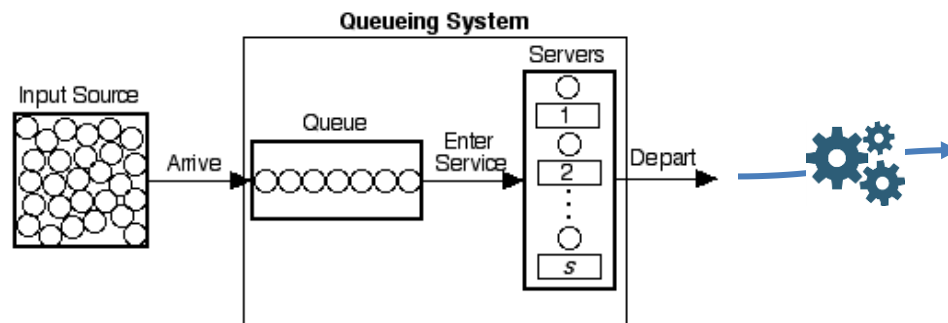


So, if simulation is a game...

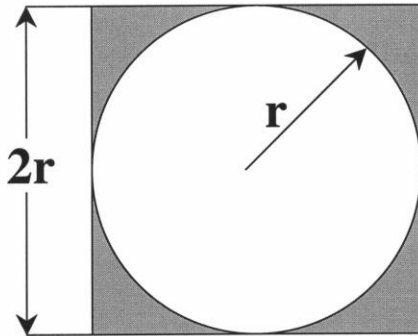
What are the rules ?



From a model to a game playing:



Static simulations – the rules



Area of Square = $4r^2$

Area of Circle = πr^2

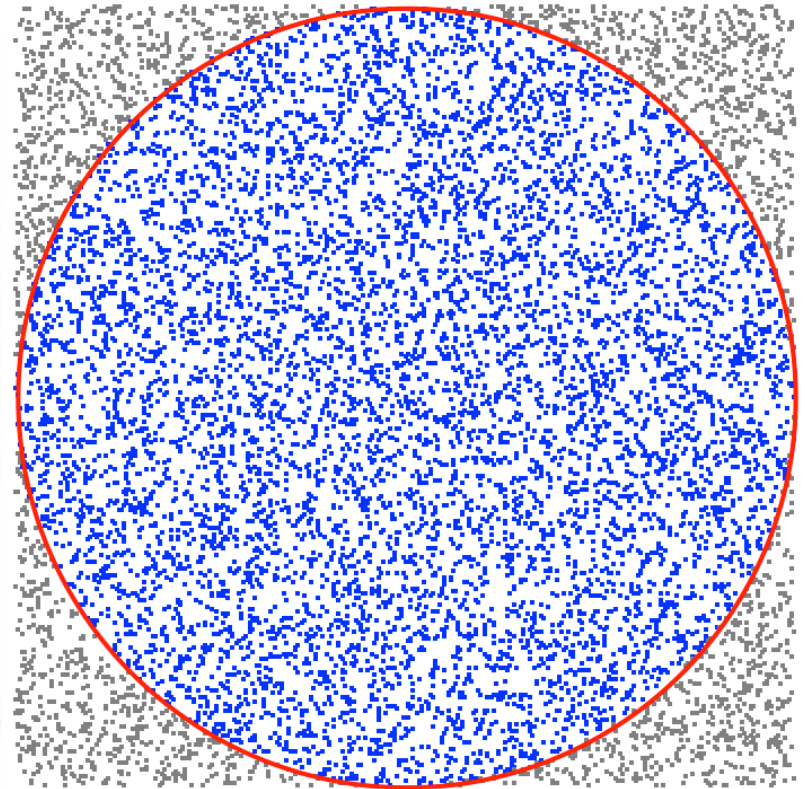
Ratio of area of Circle to area of Square = $\frac{\pi r^2}{4r^2}$
 $= \pi/4$

Total number of throws = N

No. hits inside circle = M

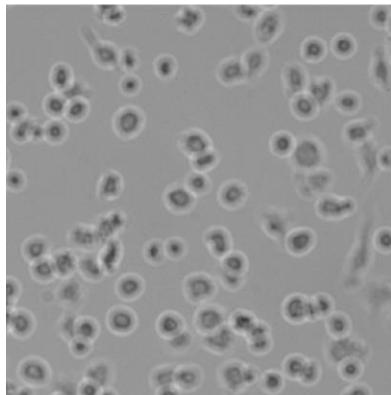
Ratio of no. hits inside circle to total no. throws = M/N

$$\pi/4 \approx M/N \Rightarrow \pi \approx 4 * M/N$$

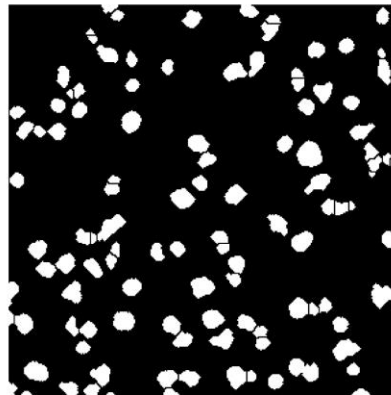


Static simulations – Playing the game

Can you play the static simulation game to calculate the density of blood cells in a sample?



Reality



Model



Simulation Engine

$x, y \rightarrow \text{random numbers}$

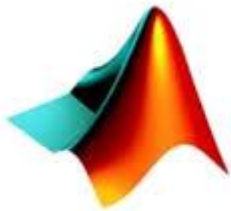


Generated !

Static simulators

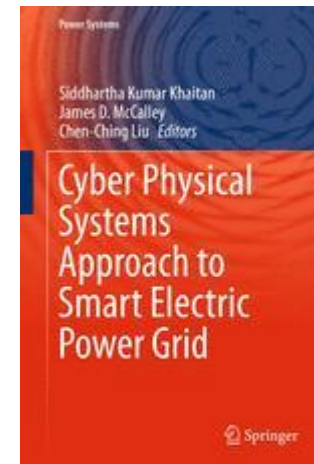
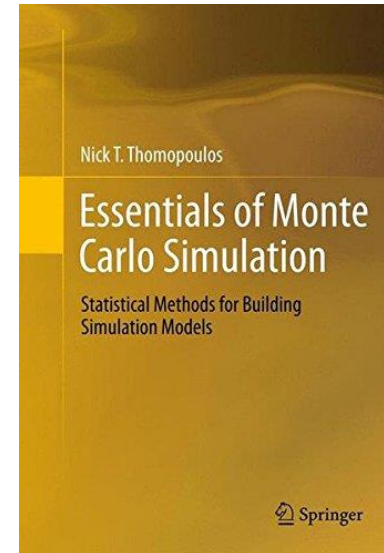


<https://www.goldsim.com>

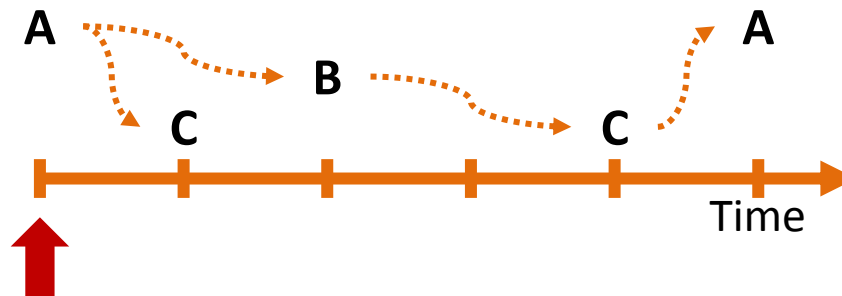
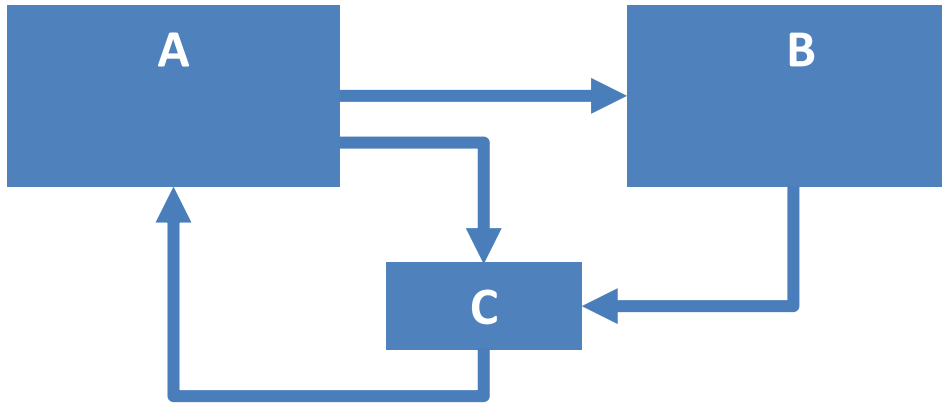


MATLAB

<https://www.mathworks.com>



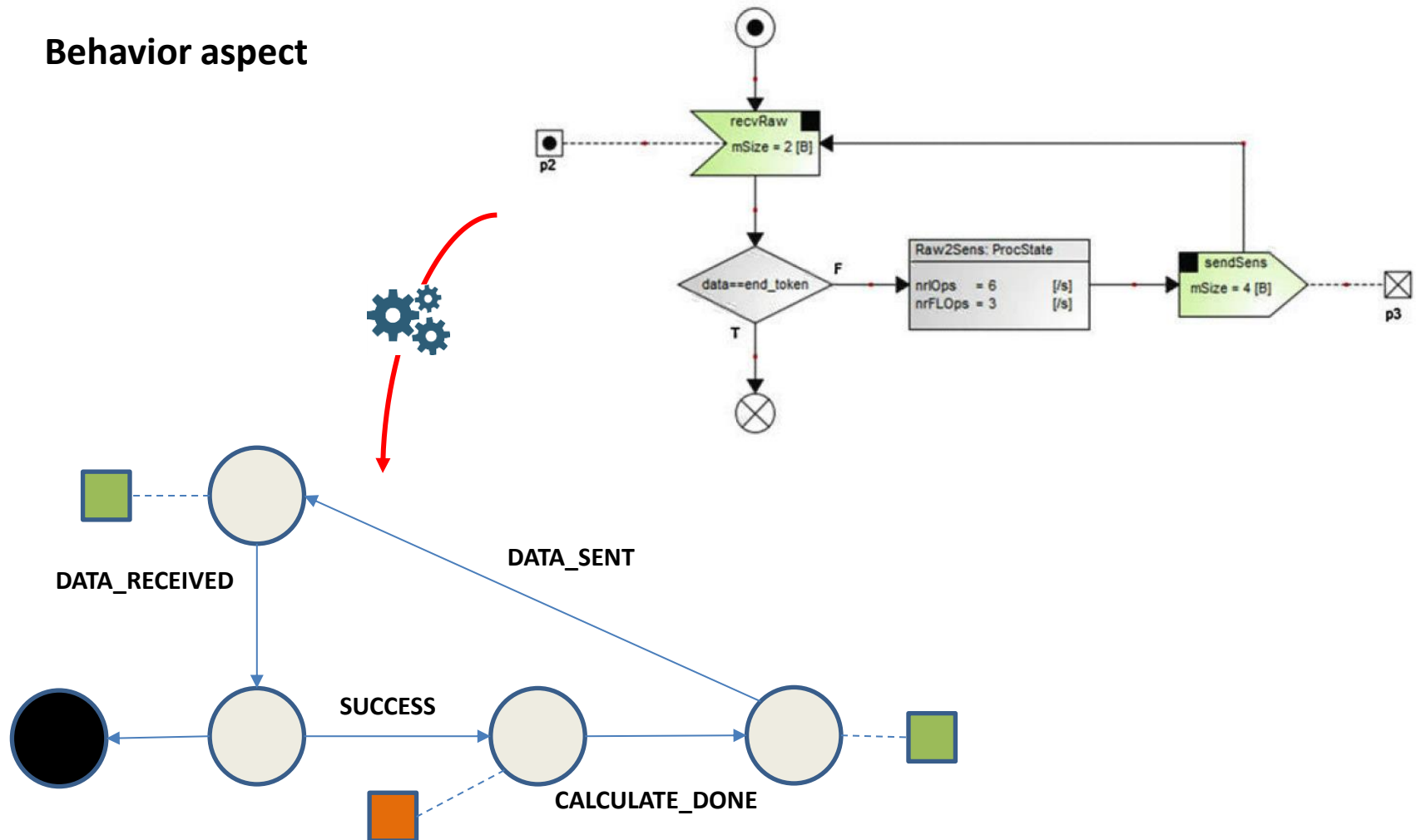
Discrete event simulation – the rules



DynAA Core (Engine)

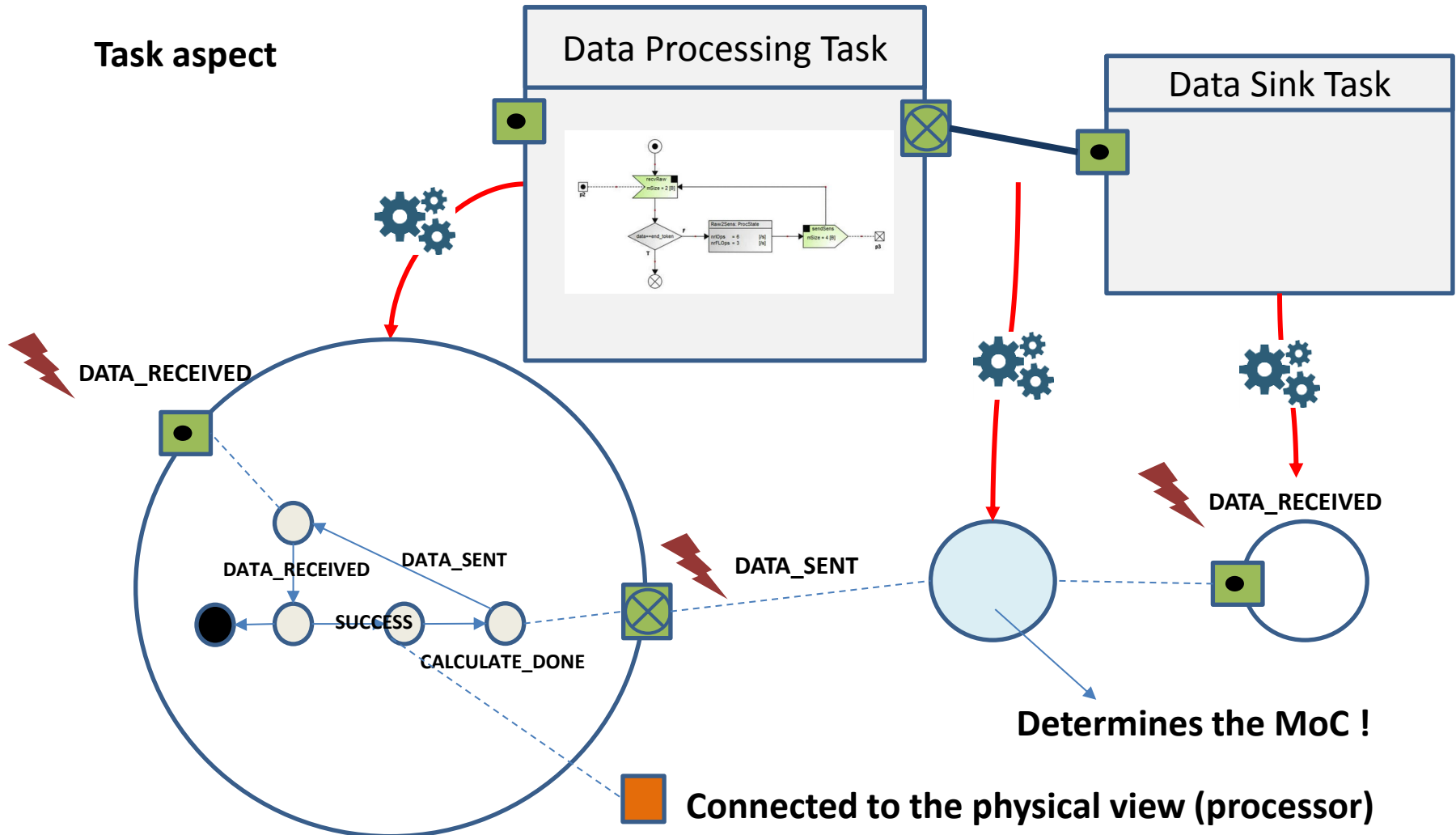
DES – Playing the game : An example from DynAA

Behavior aspect



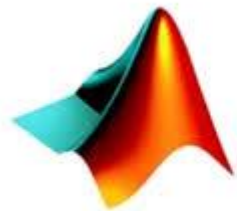
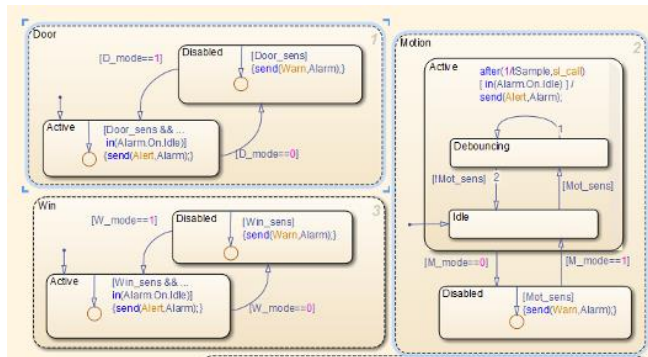
DES – Playing the game : An example from DynAA

Task aspect



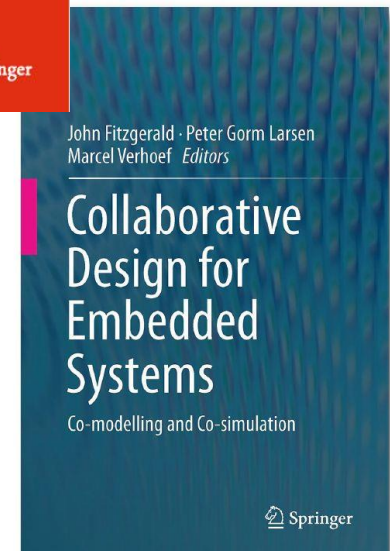
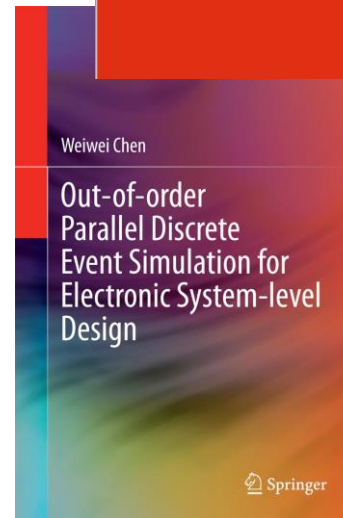
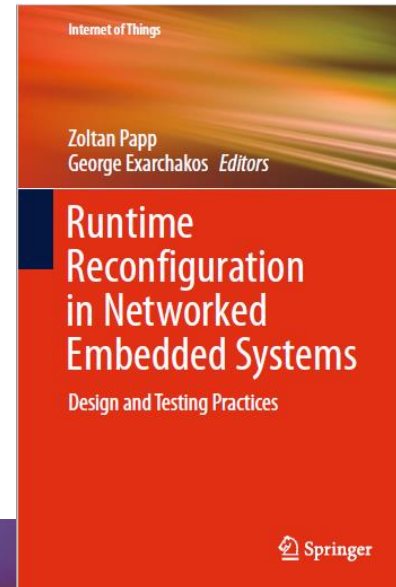
Discrete event simulators

DynAA !!!!!



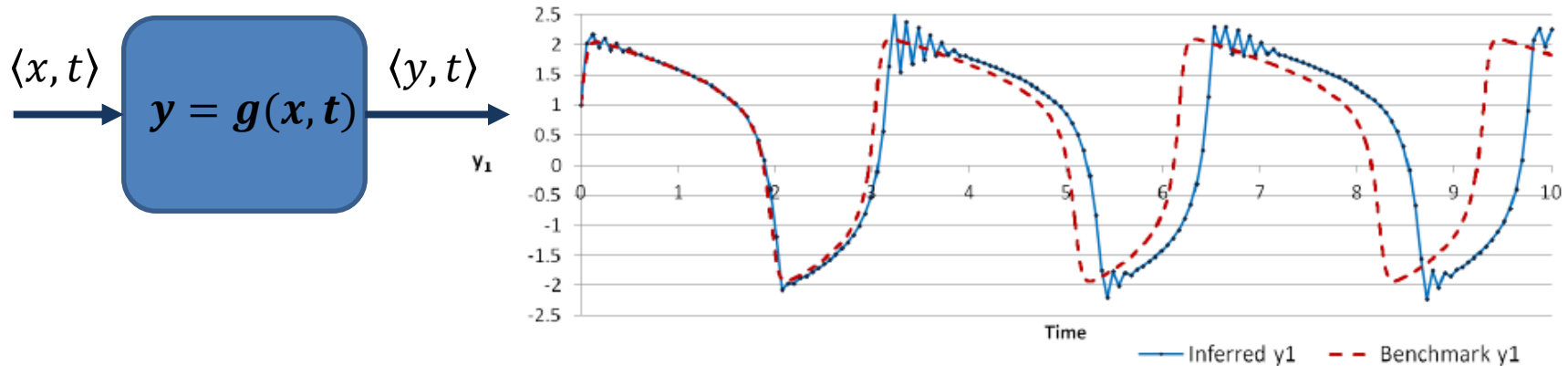
MATLAB

<https://www.mathworks.com>

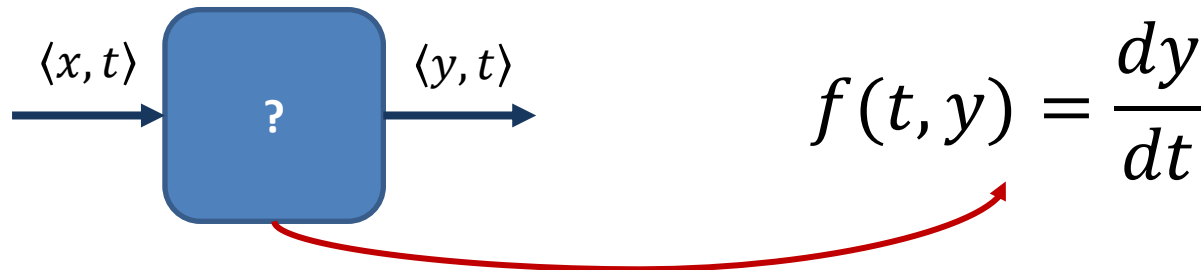


Find us Inside !

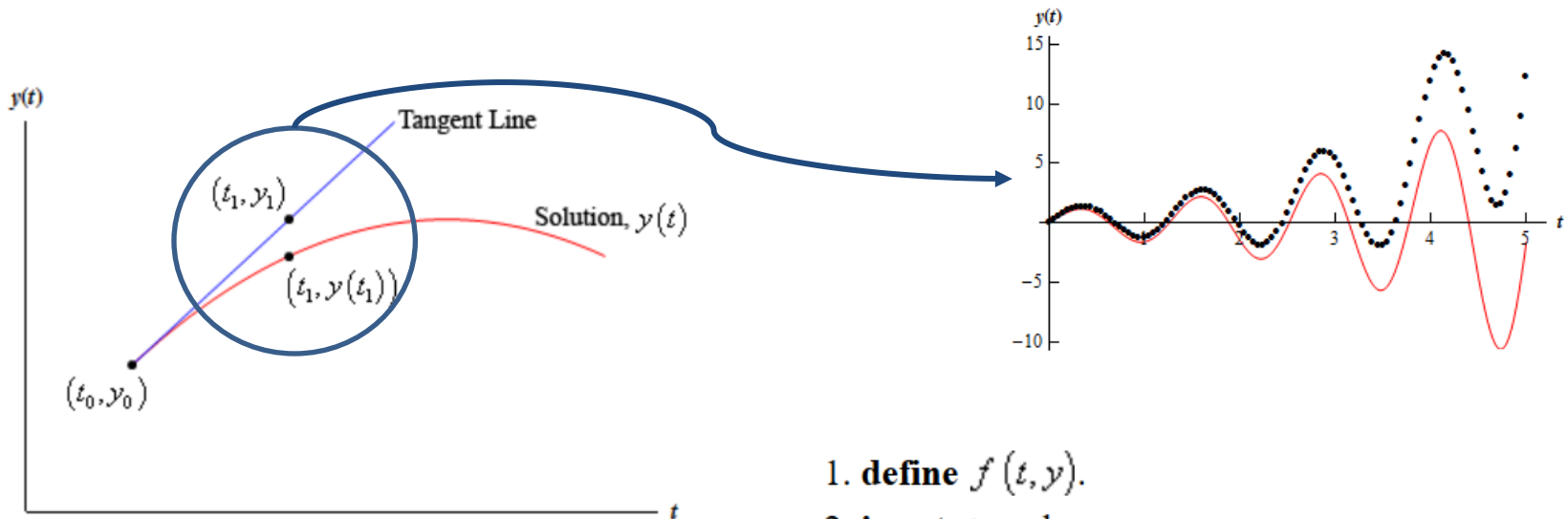
Continuous simulations – the rules



Play the game by advancing the time, step by step, and evaluating the function



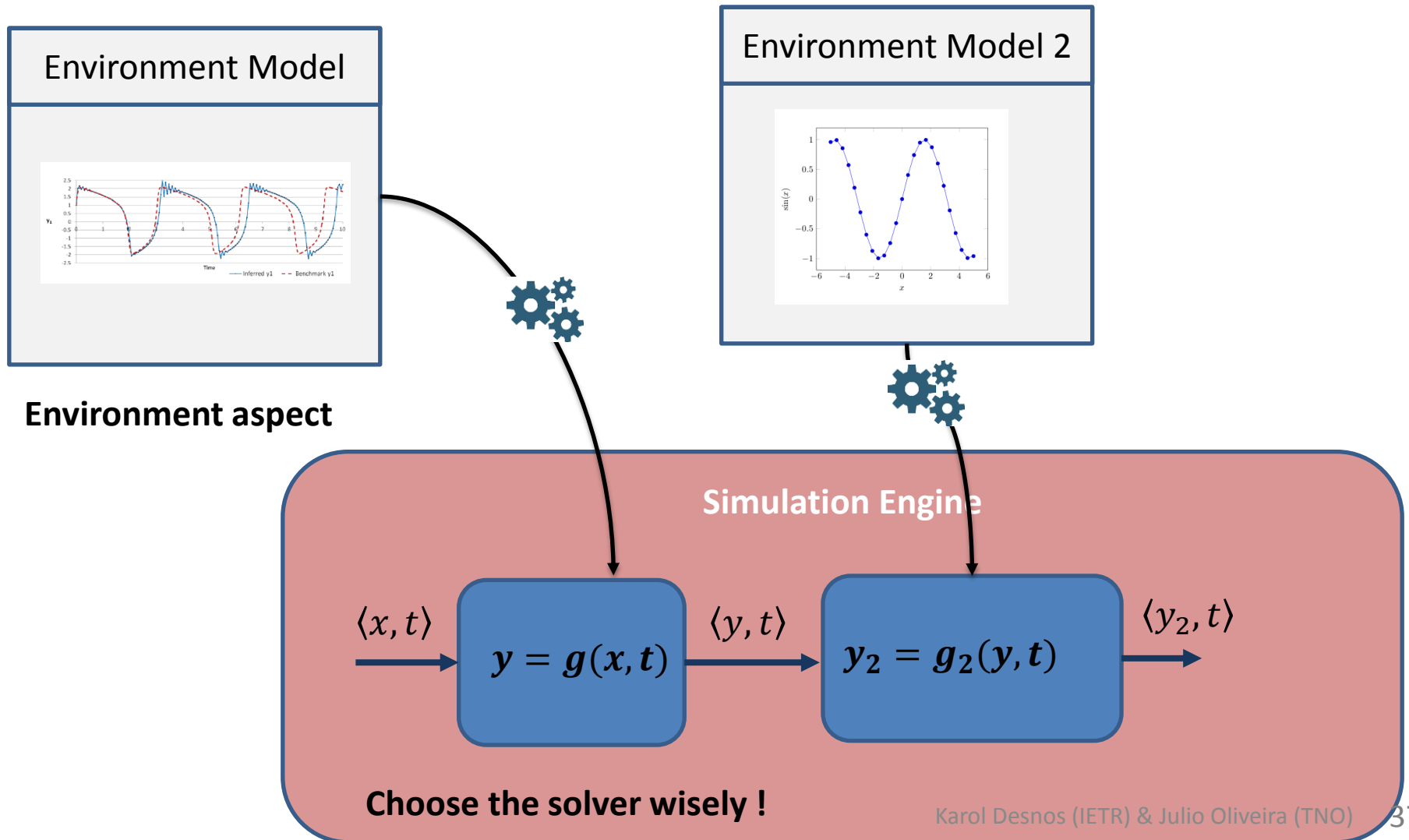
Continuous simulations – the rules



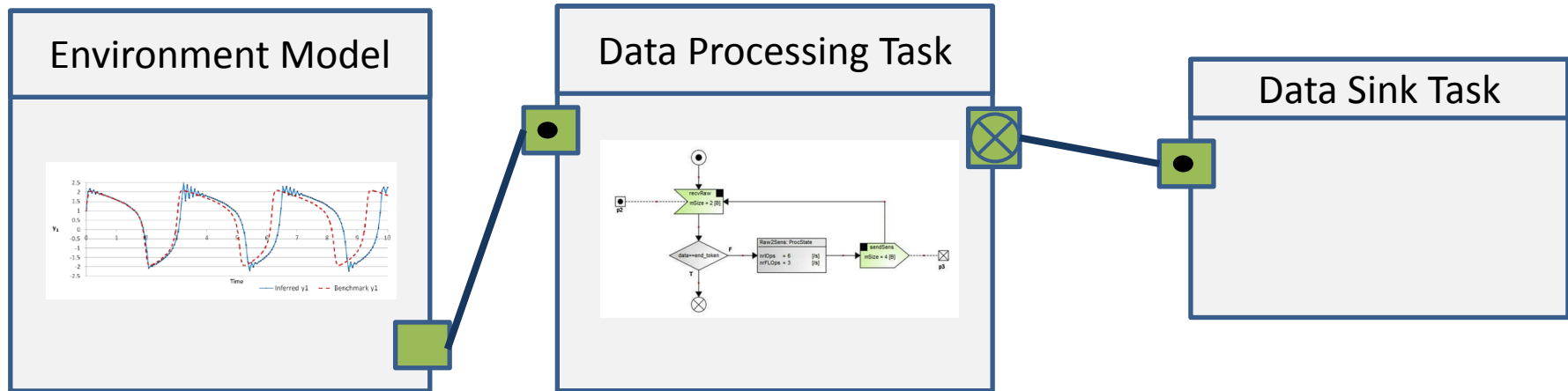
Euler's method : the simplest solver

1. **define** $f(t, y)$.
2. **input** t_0 and y_0 .
3. **input** step size, h and the number of steps, n .
4. **for** j from 1 to n **do**
 - a. $m = f(t_0, y_0)$
 - b. $y_1 = y_0 + h * m$
 - c. $t_1 = t_0 + h$
 - d. Print t_1 and y_1
 - e. $t_0 = t_1$
 - f. $y_0 = y_1$
5. **end**

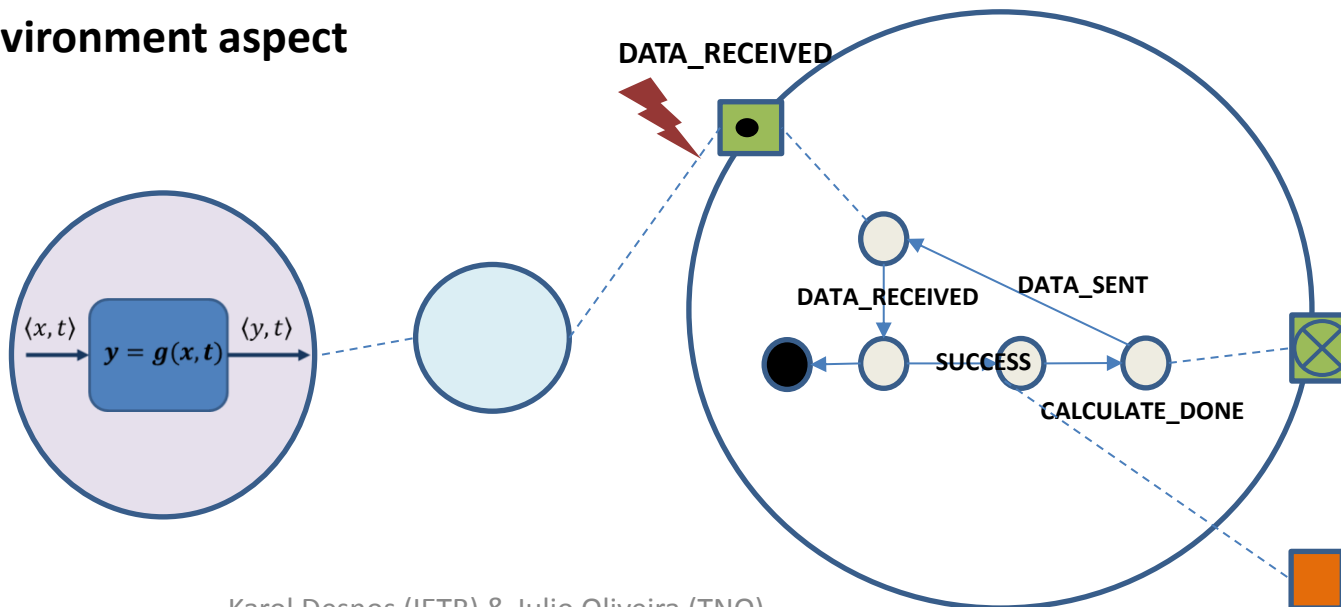
Continuous simulation – Playing the game



Short view on Hybrid simulation

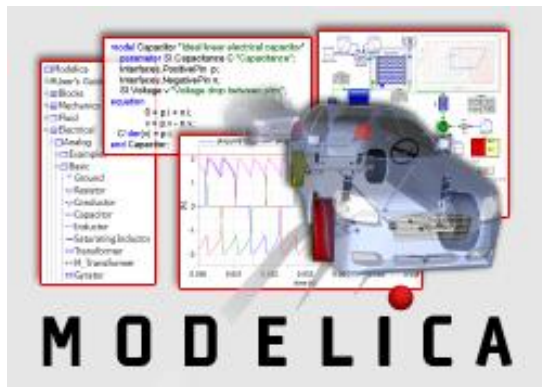


Environment aspect



Looks the same, feels the same, but much more difficult !!!

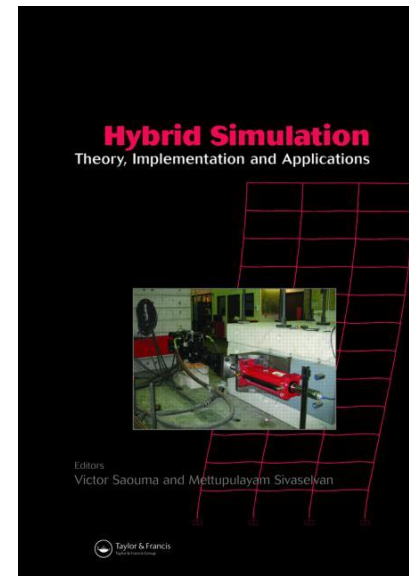
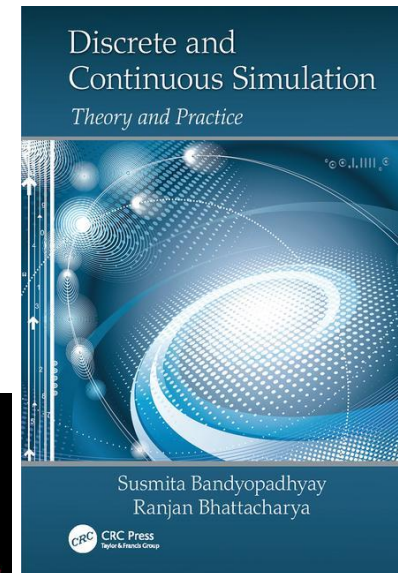
Continuous (Hybrid) simulators



<https://www.modelica.org/>



<https://www.mathworks.com>

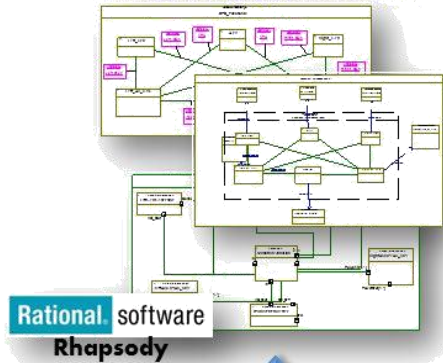


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1. Modeling Environment and Languages
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3. Simulators
4. Analysis / Optimization
5. Runtime Support

Analysis / Optimization

1. Describe system through different SysML views, including design alternatives, constraints and goals



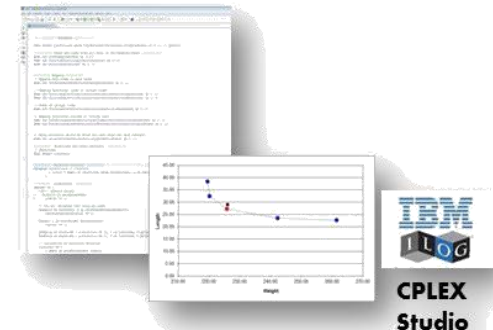
2. Derived Data Schema for Input and output structures

idname	guid	variants
1 Junction	GUID 1581-c487-4be2-9fd6-8ce56a5b32ea	Cat Junction
3 Relay	GUID 8feb223d-5bc6-40d6-b173-46c5ff3d7e58	Cat Relay

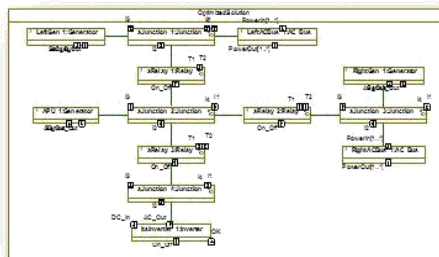
id	name	guid	typeId	type name	variants	base from to
23	Parameter	GUID 19e323c-9a0b-4902-880a-e55a3c32a2	23	Parameter	no Parameter	23 1 1
18	Generator	GUID 8a6e71a-356d-44c6-860a-f01a0b0c472	18	Generator	no Generator	18 1 1
13	Parameter	GUID a0c3970-00a-4a08-e743-d0e73887316	13	Parameter	no Parameter	13 1 1
19	Relay	GUID 82a4f2f-00a-4a08-e743-d0e73887316	19	Relay	no Relay	19 1 1
25	PU	GUID 141030a-74a4c5-4902-e4a02a5b0883	25	Parameter	no PU	25 1 1
8	Converter	GUID 33a0b88-3309-4a08-e743-d0e73887316	8	Converter	no Converter	8 1 1
10	Relay	GUID 1230b88-3309-4a08-e743-d0e73887316	10	Relay	no Relay	10 1 1
21	Parameter	GUID 3e20f00-8914-4a08-e743-d0e73887316	21	Parameter	no Parameter	21 1 1
13	Relay	GUID 8881a19-95d-4a08-e743-d0e73887316	13	Relay	no Relay	13 1 1
14	Relay	GUID 8881a19-95d-4a08-e743-d0e73887316	14	Relay	no Relay	14 1 1
23	Parameter	GUID a0c3970-00a-4a08-e743-d0e73887316	23	Parameter	no Parameter	23 1 1

Architecture
Optimization
through Design
Space Exploration
iterations

3. Automatic translation(via an interchange format) into Optimization solver



4. Optimized architecture back annotated to SysML model



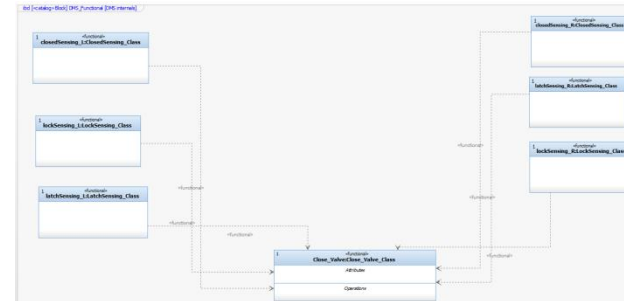
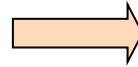
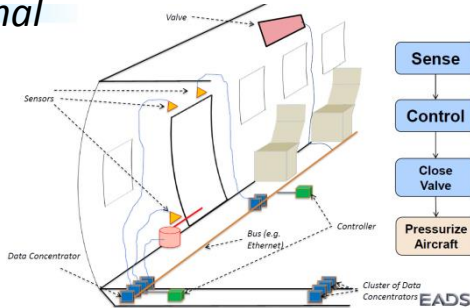
Development and Analysis of a Simplified Doors Control System



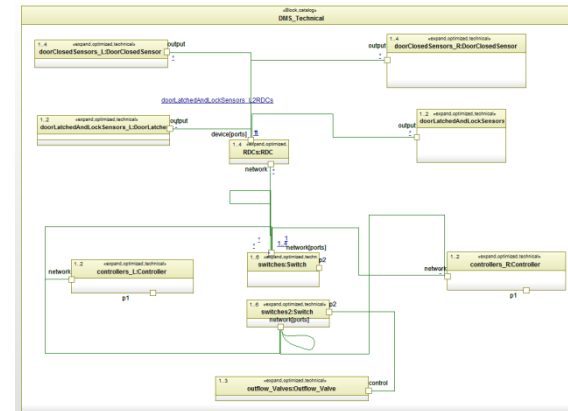
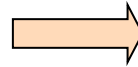
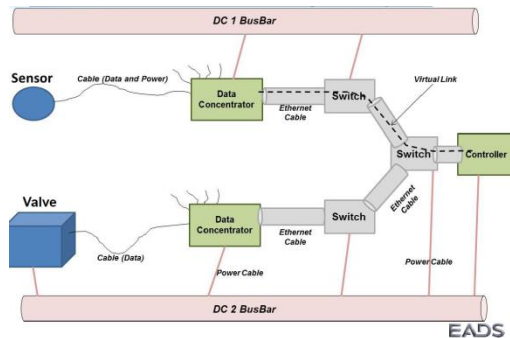
- Monitor and Control Passenger Doors, Emergency Exits, and Cargo Doors
- Design a system out of existing components for best weight, cost, power etc.

From user story to model

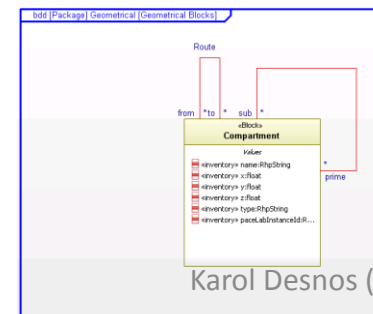
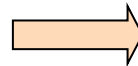
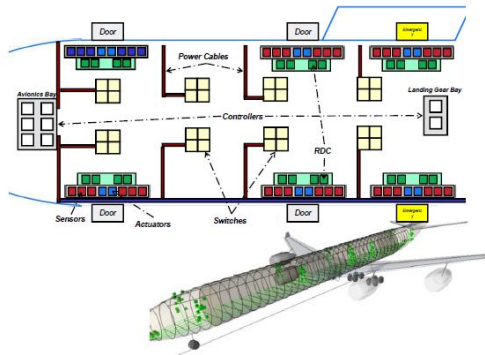
Functional



Technical

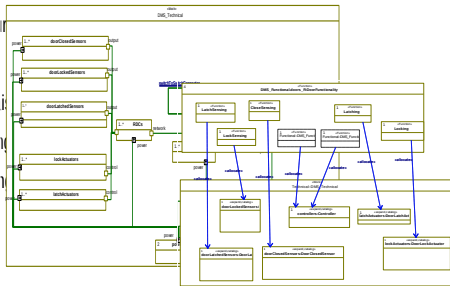


Geometrical

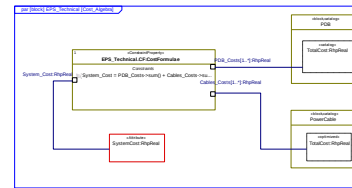


Optimization Auto-Generation

- P1: whenever [E] occurs [SC] holds during following [I]
P2: whenever [E1] occurs [E2] implies [E3] during following [I]
P3: whenever [E1] occurs [E2] does not occur during following [I]
P4: whenever [E] occurs [E/SC] occurs during following [I]
P5: [SC] during [I] raises [E]
P6: [E1] occurs [N] times during [I] raises [E]
P7: [E] occurs at most [N] times during [I]
P8: [SC] during [I] implies [SC1] during [I1]



- *Objectives*



- *Component library*

[illegible]

- Automatic Generation

■ Requirements & Constraints

- *Optimization Problem Formulation (CPLEX)*

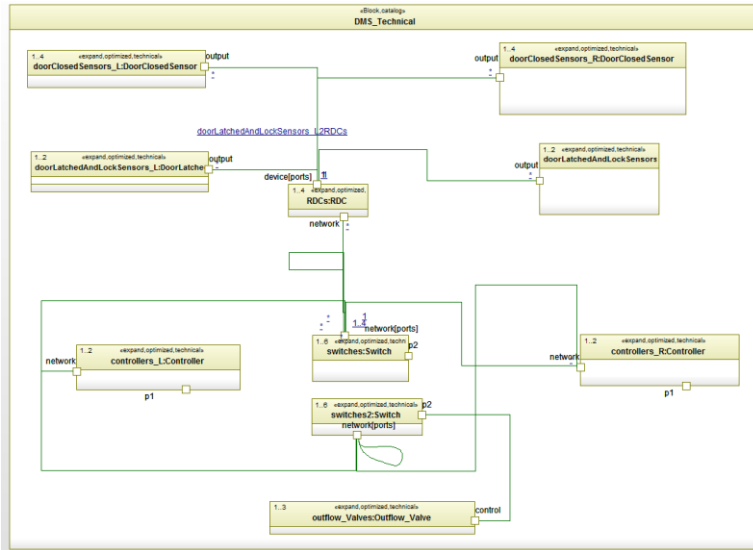
```

// declare dependencies // include <algorithm> // include <iostream>
using namespace std;
int main() {
    int n;
    // read input
    cin >> n;
    // initialize array
    vector<int> arr(n);
    // read input
    for (int i = 0; i < n; i++) {
        cin >> arr[i];
    }
    // sort array
    sort(arr.begin(), arr.end());
    // print array
    for (int i = 0; i < n; i++) {
        cout << arr[i] << " ";
    }
    return 0;
}

```

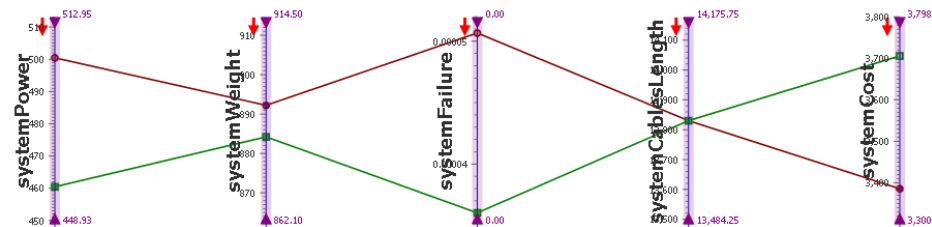


1. SysML modeling

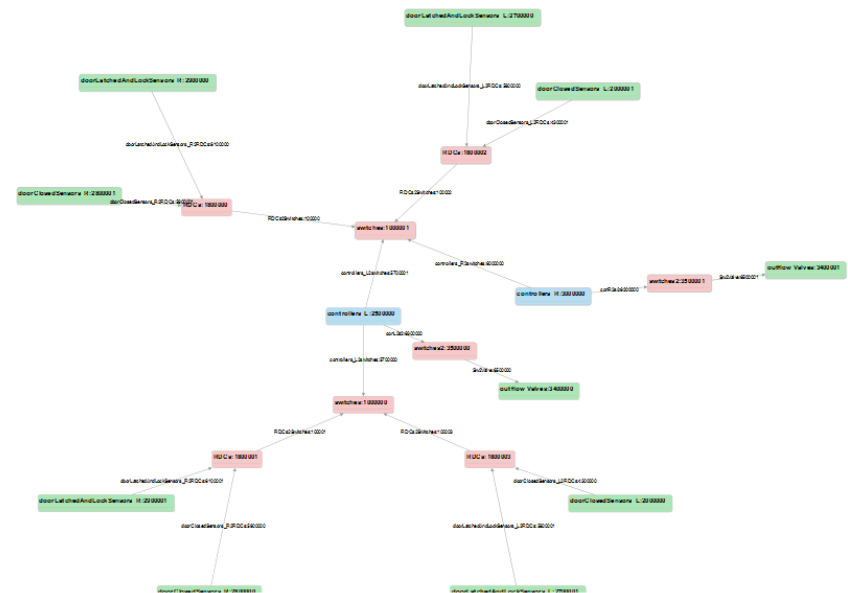
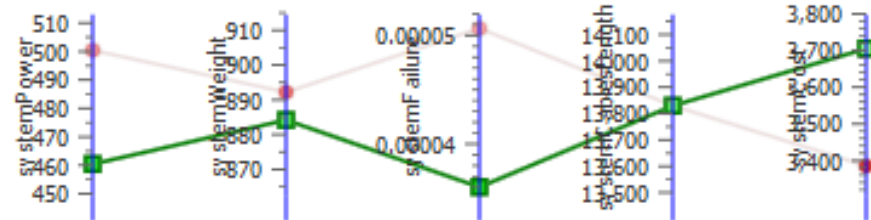


2. Run Optimization and show alternatives

ID	systemPower	systemWeight	systemFailure	systemCablesLength	systemCost	Finished at	Duration
2e937c-a4b9-4ac8-b0ab-702de3a1c94a	500.44	892.20	5.066E-5	13830.00	3385.50	May 23, 2013 11:14:54 AM	942 sec
3232cbf2-0383-4500-811a-52d643079cd3	460.44	884.20	3.602E-5	13830.00	3705.50	May 23, 2013 11:10:54 AM	938 sec



Results



HW/SW Cyber-System Modeling Tools

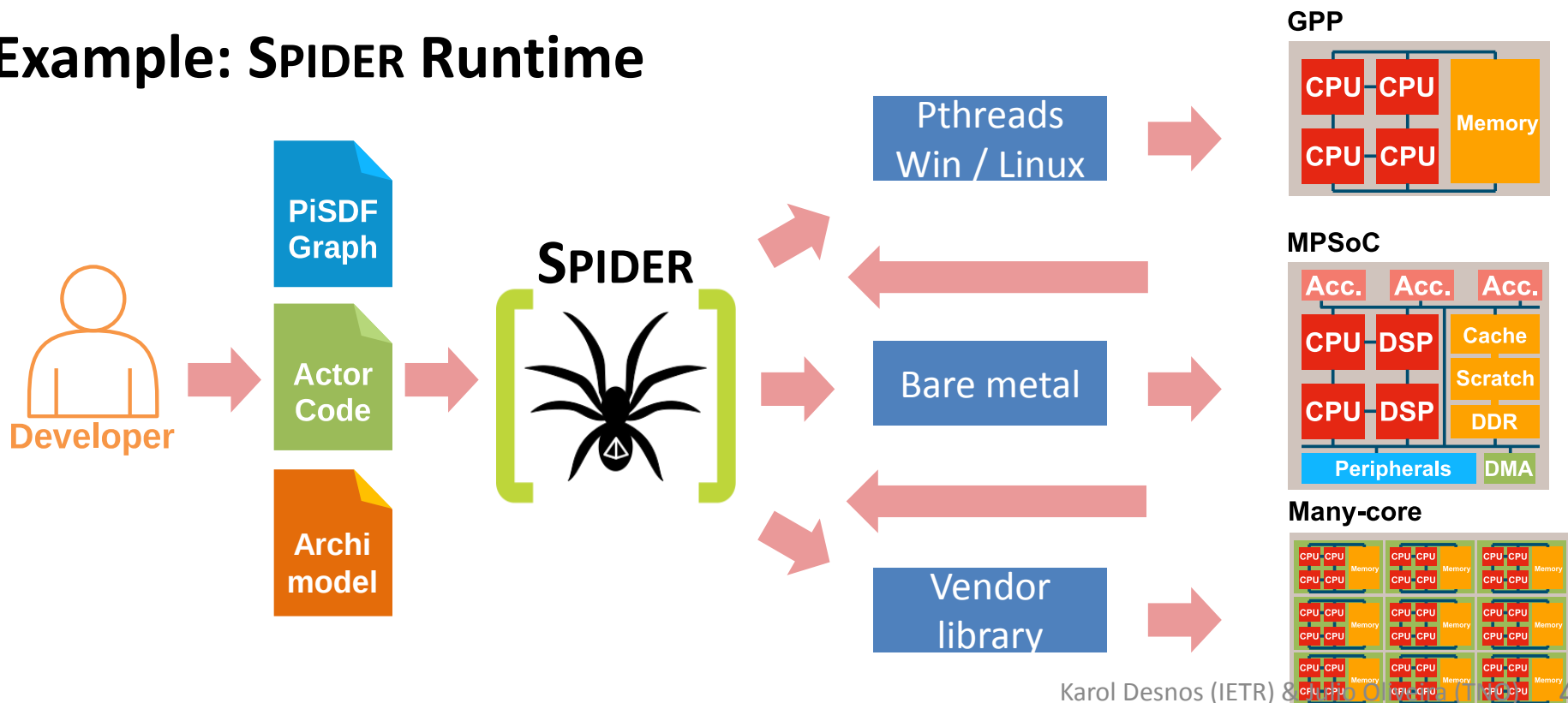
1. Modeling Environment and Languages
2. (HW &) SW Synthesis
3. Simulators
4. Verification / Validation
5. Runtime Support

Overview

Runtime adaptation layer:

- Services needed to run an application
- Provided by “classic” OS, and/or model-aware utilities.

Example: SPIDER Runtime



Different Runtime Strategies

Adaptivity++

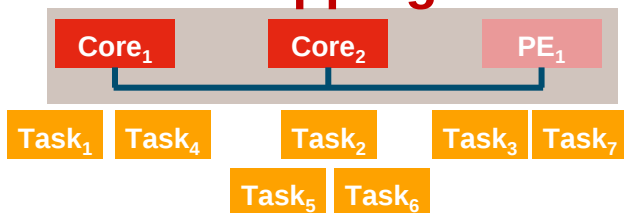


	Mapping	Scheduling	Timing
fully dynamic	run	run	run
static-assignment	compile	run	run
self-timed	compile	compile	run
fully static	compile	compile	compile

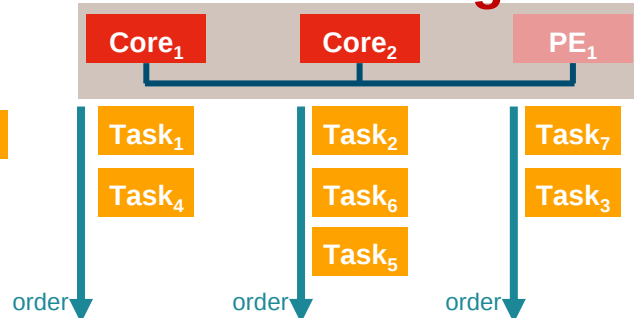


Performance++

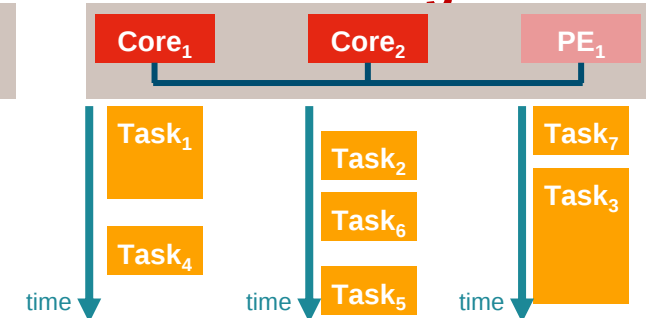
Mapping



Scheduling



Timing



Fully static runtime support

Computation

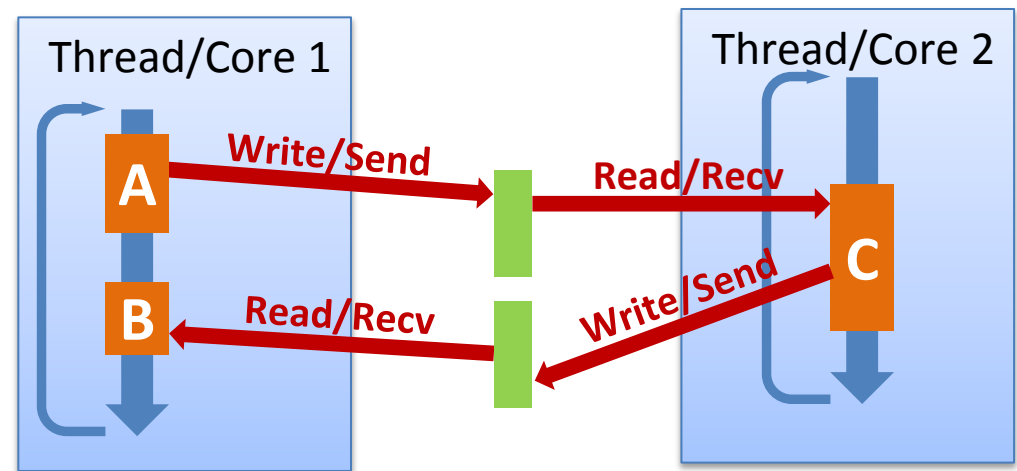
- Non-preemptible processes/threads
- Bare-metal or real-time OS
- Global clock

Communications

- Non-blocking

Used for:

- Hard Real-time systems



Self-timed runtime support

Computations

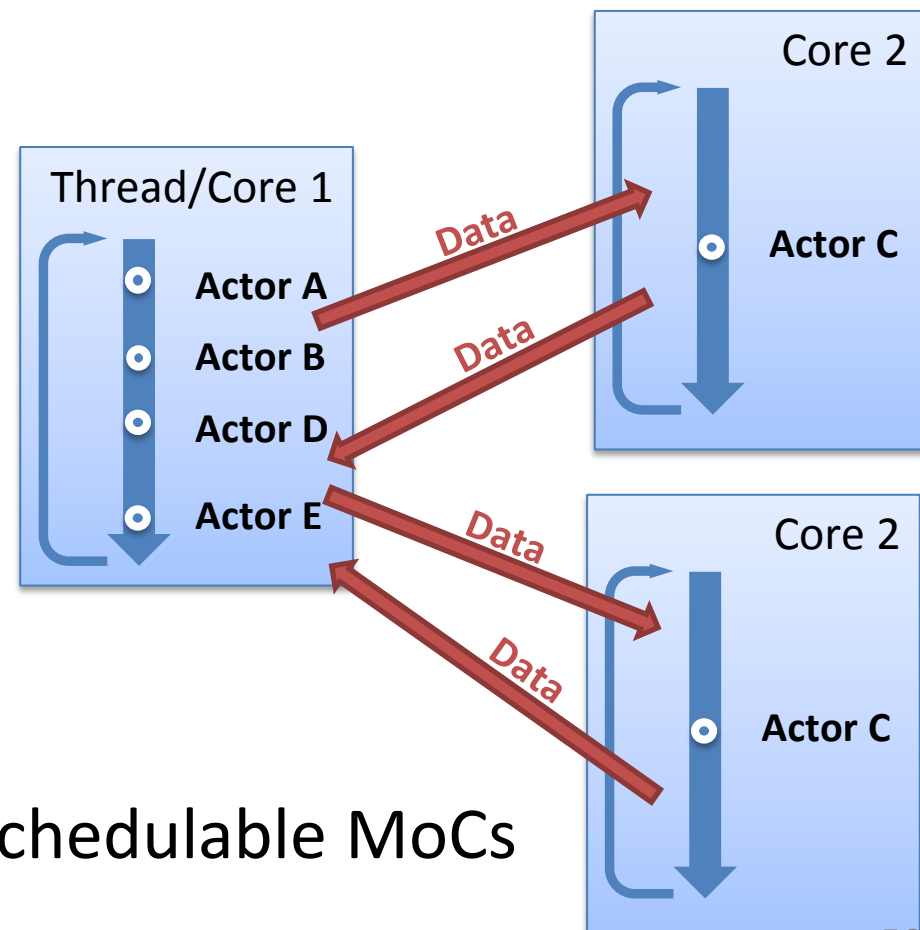
- Processes/threads/tasks
- Bare-metal or OS

Communications

- Blocking
- Synchronization mechanism:
Barrier, Mutexes,
Semaphores, ...

Used for/by:

- Real-time systems, statically schedulable MoCs
- E.g. Preesm, Syndex



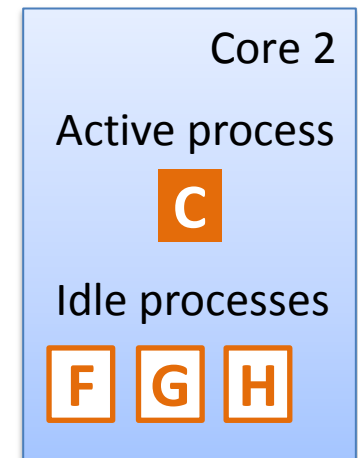
Static assignment runtime support

Computations

- Processes/threads/tasks
- OS with **scheduler**

Communications

- Blocking
- Synchronization mechanism:
Barrier, Mutexes,
Semaphores, Yield...



Used for/by:

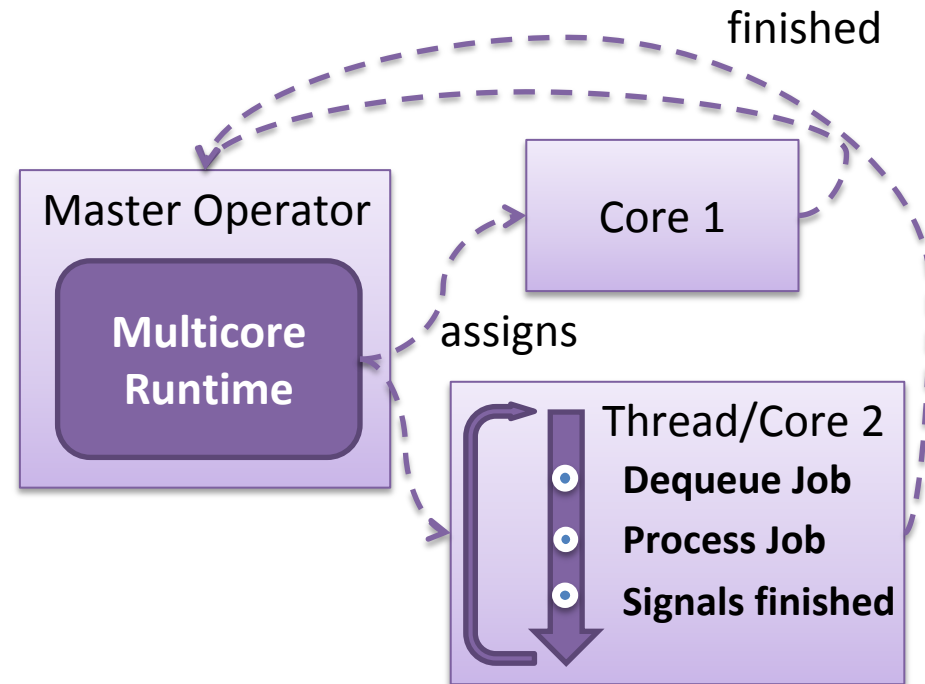
- Dynamic/Reconfigurable models (e.g. Kahn Process Network)
- E.g. Open RVC-CAL Compiler (ORCC), PaDaF

Fully dynamic runtime supports

Master/Slave model

- Pros:
 - Adaptivity
 - Controlled decisions
 - Compatible with heterogeneous target
- Cons:
 - Master overhead
 - Master bottleneck

Master/Slave
(e.g. Spider Runtime)

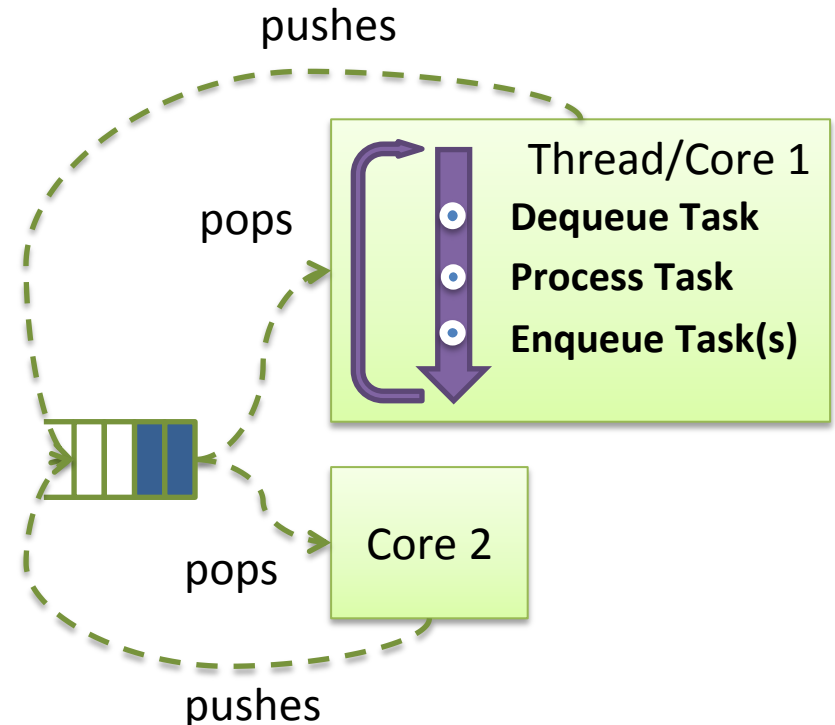


Fully dynamic runtime supports

Work queuing

- Pros:
 - Adaptivity
 - Light/No Overhead
- Cons:
 - Shared queue bottleneck
 - No “intelligence”
 - Non-determinist

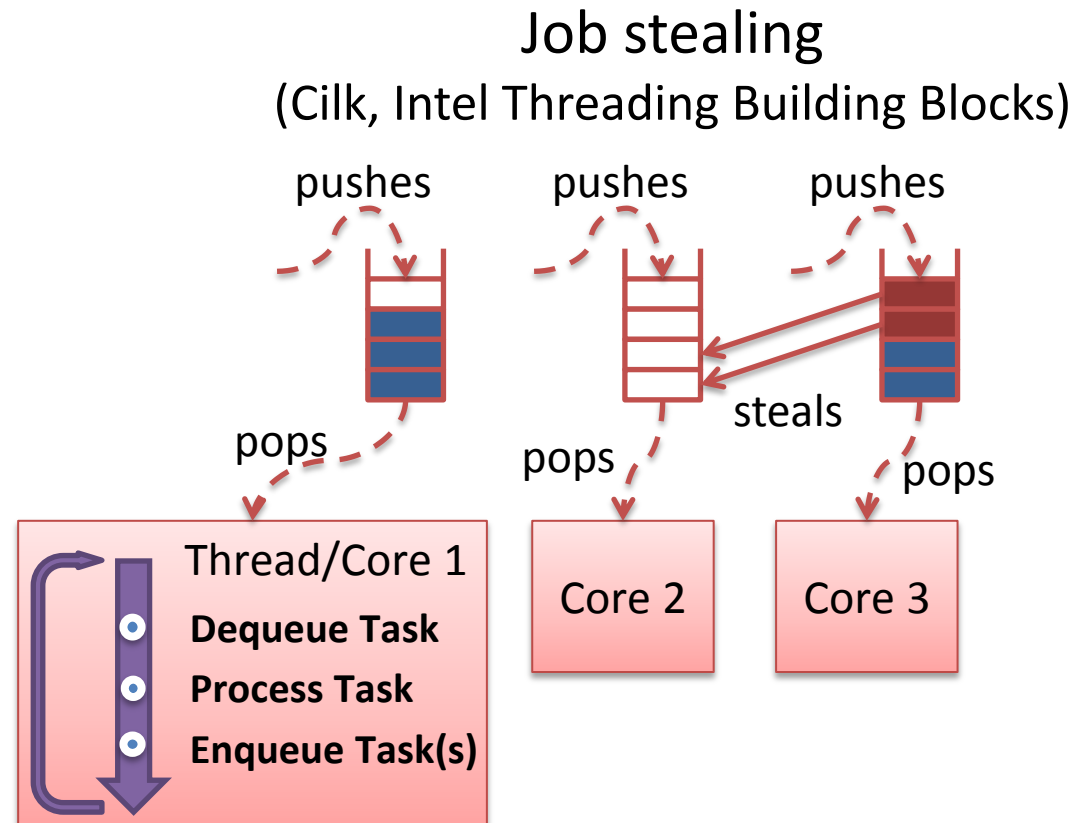
Work-queueing
(Apple Grand Central Dispatch, OpenMP)



Fully dynamic runtime supports

Job Stealing

- Pros:
 - Adaptivity
 - Light/No Overhead
 - No bottleneck
- Cons:
 - No “intelligence”
 - Non-determinist



Final words

AN x64 PROCESSOR IS SCREAMING ALONG AT BILLIONS OF CYCLES PER SECOND TO RUN THE XNU KERNEL, WHICH IS FRANTICALLY WORKING THROUGH ALL THE POSIX-SPECIFIED ABSTRACTION TO CREATE THE DARWIN SYSTEM UNDERLYING OS X, WHICH IN TURN IS STRAINING ITSELF TO RUN FIREFOX AND ITS GECKO RENDERER, WHICH CREATES A FLASH OBJECT WHICH RENDERS DOZENS OF VIDEO FRAMES EVERY SECOND

BECAUSE I WANTED TO SEE A CAT
JUMP INTO A BOX AND FALL OVER.



I AM A GOD.