



HW/SW Cyber-System Co-Design and Modeling

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Who are we?







Julio de Oliveira

Position:

TNO - Researcher & innovation scientist

Topic of interest:

 Large, distributed, and autonomous systems

Karol Desnos

Position:

- INSA Rennes Assoc. Prof.
- IETR Researcher

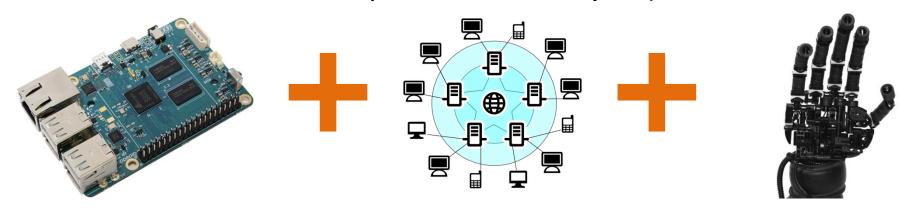
Topic of interest:

- Dataflow Programming
- Embedded MPSoCs



Text-book definitions for Cyber-Physical Systems:

- CPS are complex systems integrating:
 - Computation processes
 - Network of communication
 - Physical entities (actuators and sensors, time, mechanics, temperature, ..., and you!)



 CPS is an engineering discipline, focused on technology, with a strong foundation in mathematical abstractions.



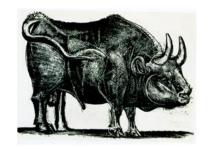


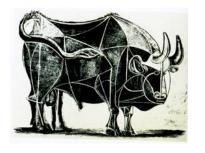
Abstraction?

Tradeoff between level of details and complexity.



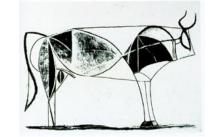


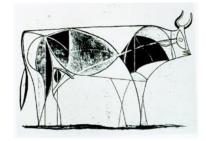






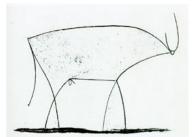












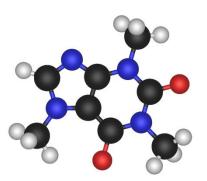
Picasio



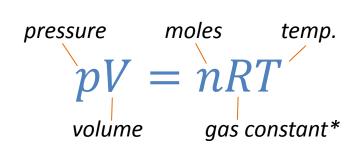
What is a model?

- Abstract (mathematically grounded) representation capturing predictable characteristics of a "system".
- Models for similar constituents may take many forms.
 - To capture different characteristics.
 - To be more suitable for a different system size.

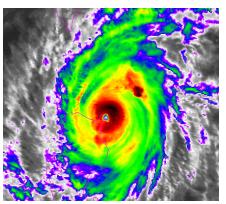
Molecules



Ideal Gas Law



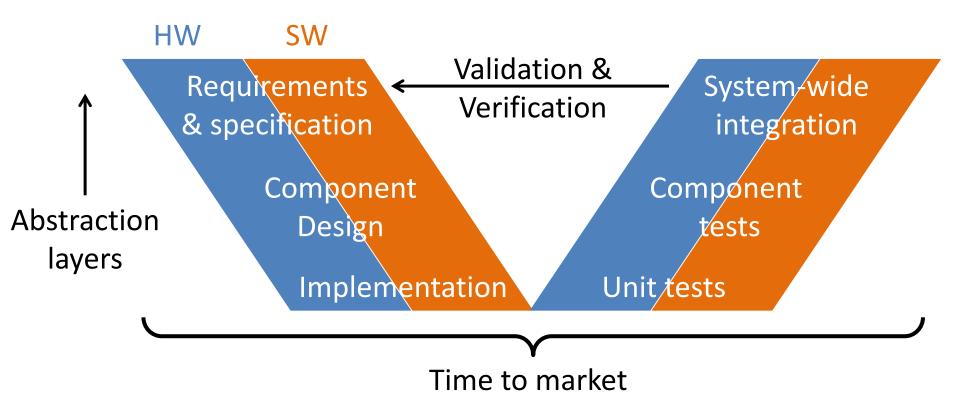
Meteorology





CPS Co-Design?

"Old" embedded system co-design flow:



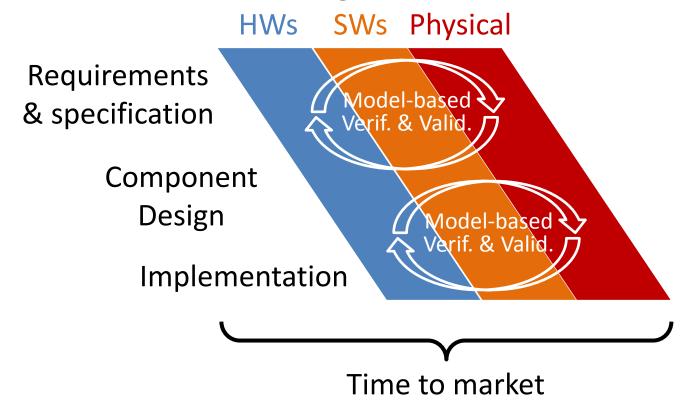
Where are physical concerns?





CPS Co-Design?

Model-based CPS co-design flow:



Models enable: system assessment, system validation & verification, (automated) system implementation.



CPS design is complex

- Many building blocks,
- Separate but intricate optimization objectives,
- Many design constraints.
 - Application Constraints
 - Real-time requirements
 - Reliability constraints
 - Limited size and power

- Cost Constraints
 - Engineering cost
 - Production cost

- External Constraints
 - Regulation and Standards
 - Environmental constraints





Course objective

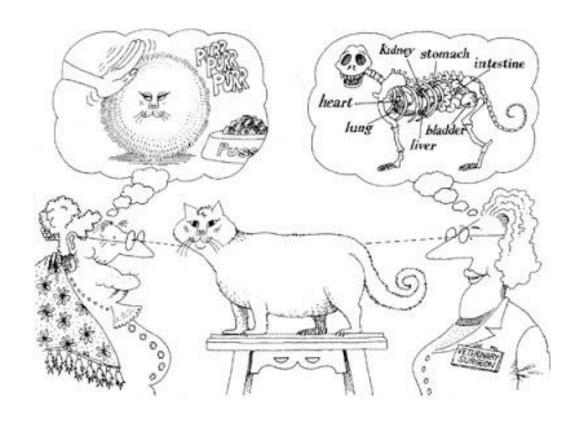
- 1. HW/SW Cyber-System Co-Design and Modeling Get a sense of how, why, and which models are used at different levels and steps of CPS design.
- 2. HW/SW Cyber-System Modeling Tools
 What do tools do to (automatically) build actual
 CPS systems from abstract models.







Modeling as an engineering activity



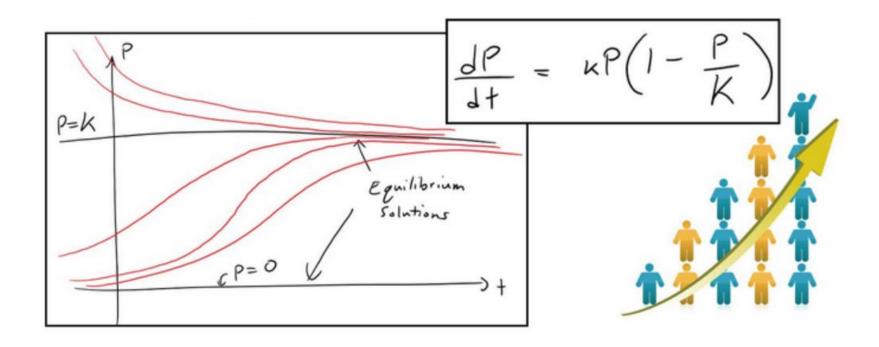
Abstraction (Simplification)

Description (Specification)

Operational (Executable)



Modeling – Example





Why modeling CPS (SoS) is challenging?



Which abstraction?

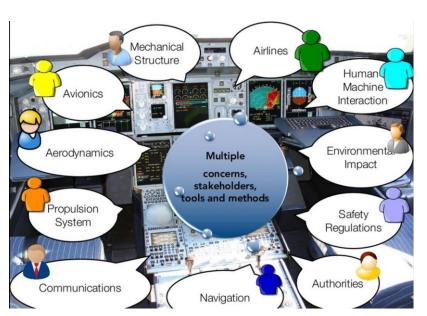
How to describe?

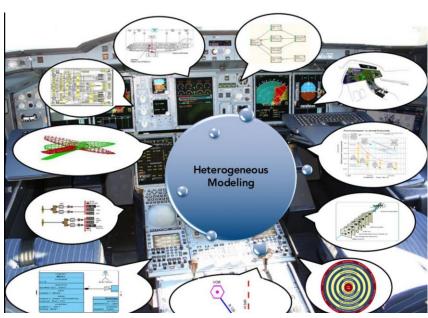
Operational?

Complexity!



What we mean by complexity?



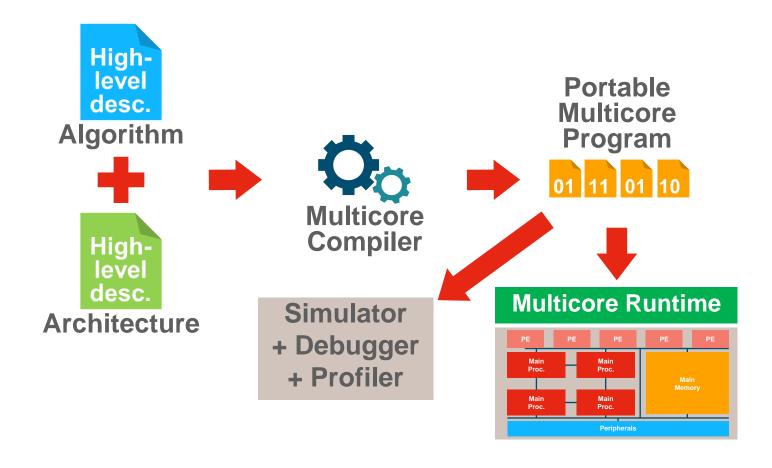




Source: INRIA

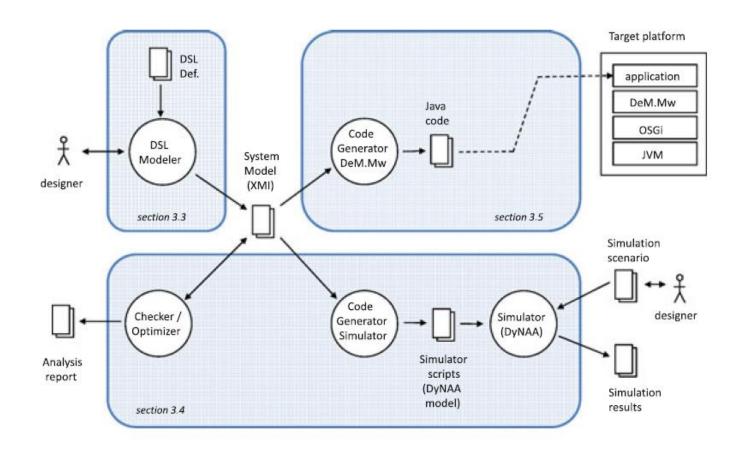


Why bother?



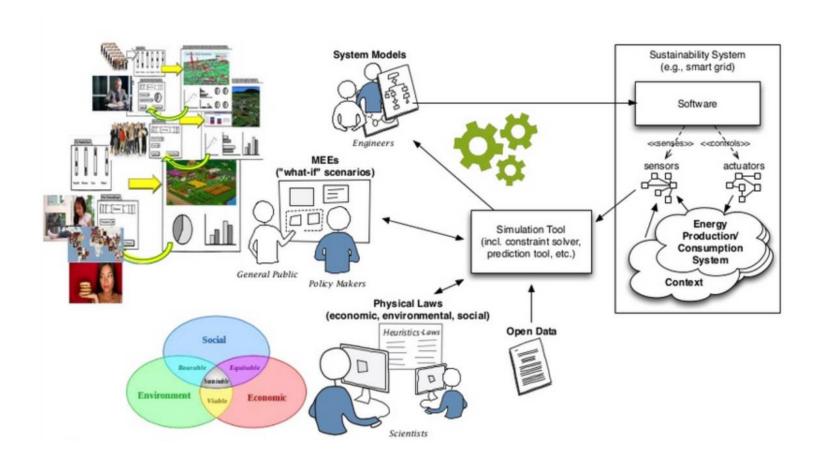


Why bother?





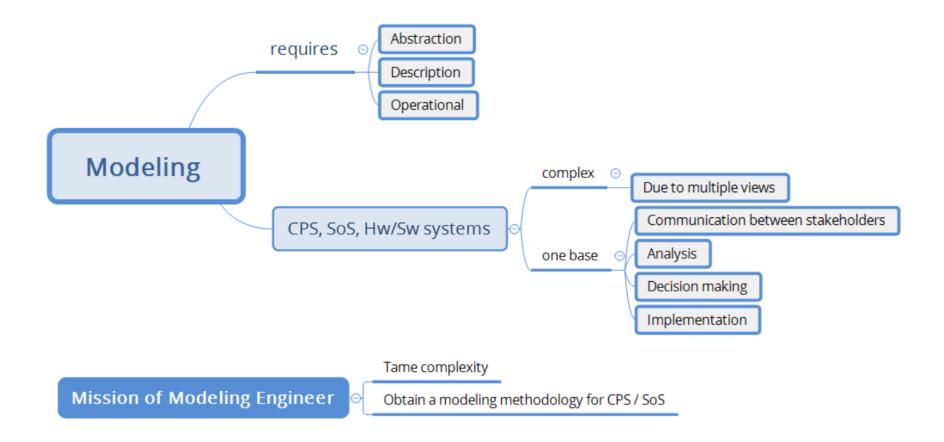
Why bother?



Source: INRIA



In a nutshell

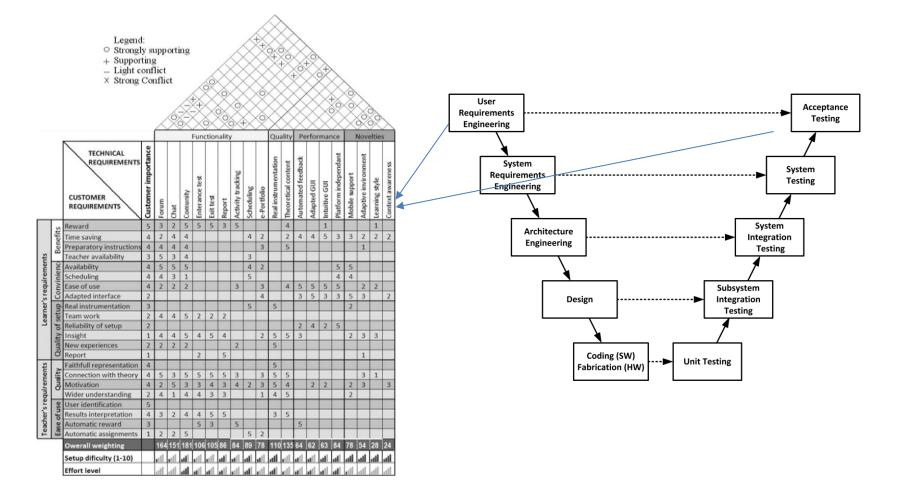




Ways to approach system level modeling

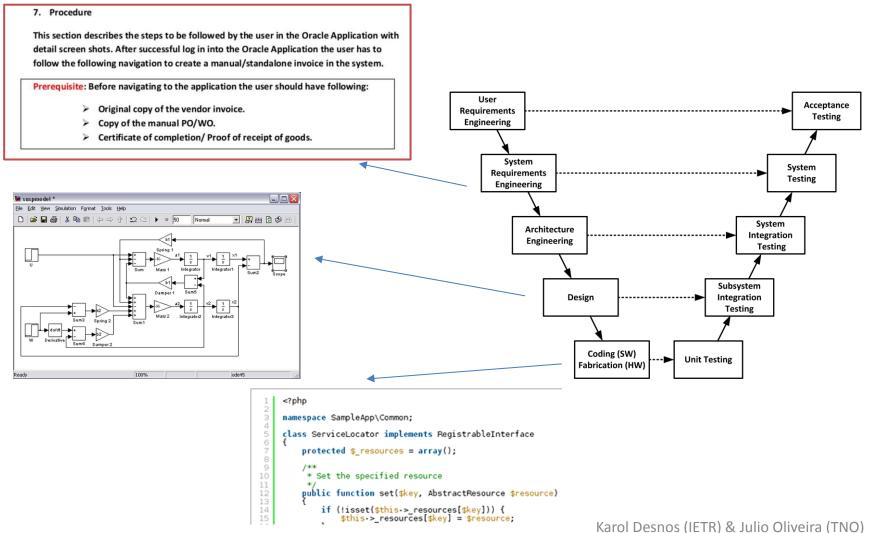


Approach 1: Model for the task in hand



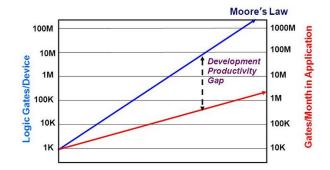


Approach 1: Model for the task in hand





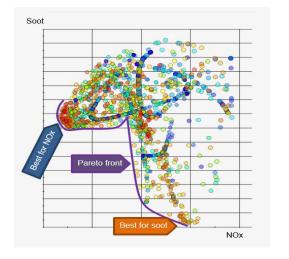
Model for the task in hand fails



Major problem for the development productivity



Introduction of errors : Human failure or mis-interpretation



Almost impossible to optimize at system level



Approach 2: Model transformation

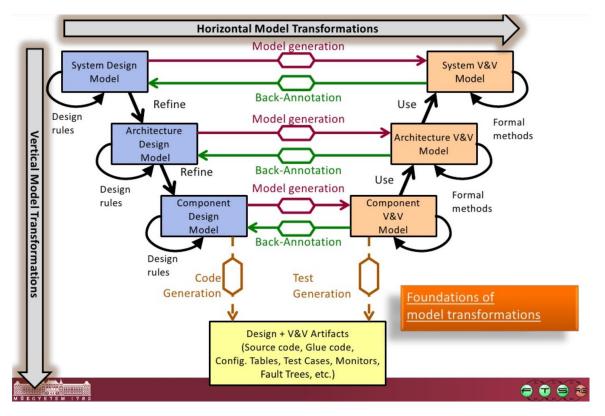
A model transformation is an automated way of modifying and creating models.

(Best) Example: Compilers

```
Analyse View
                                     @ X C++
Instructions
8048094:
           push
                      ebp
8048095:
           mov
                      ebp, esp
                                           int32 t gcd(int32 t arg1, int32 t arg2)
8048097:
           sub
                      esp, 0x18
                                             int32 t eax1;
804809a:
                      [ebp + 0xc]:32, 0x0
           cmp
804809e:
          inz
                      0x80480a5
                                             if (arg2 != 0) {
80480a0:
                      eax, [ebp + 0x8]:32
          mov
                                                eax1 = gcd(arg2, arg1 % arg2);
80480a3:
                      0x80480c1
           imp
                                               else
                                                eaxl = argl
80480a8:
                      edx, eax
80480aa:
                      edx, 0x1f
                                             return eaxl:
80480ad:
                      [ebp + 0xc]:32
80480b0:
          mov
                      eax, edx
80480b2:
                      [esp + 0x4]:32, eax
80480b6:
                      eax, [ebp + 0xc]:32
           mov
80480b9:
                      [esp]:32, eax
           mov
                      0x8048094
80480bc:
           call
80480c1:
           leave
80480c2:
                         Assembly Code
                                                                  Source Code
Line 6, Column 27
```



Model transformation and the design process



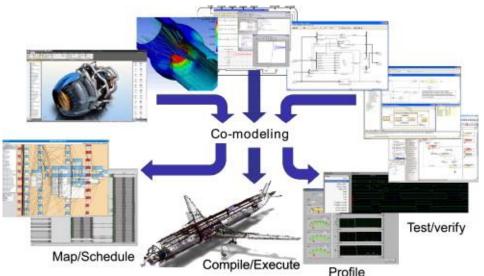
Source: Daniel Varro, CSMR2012



Approach 3: Multi-aspect modeling

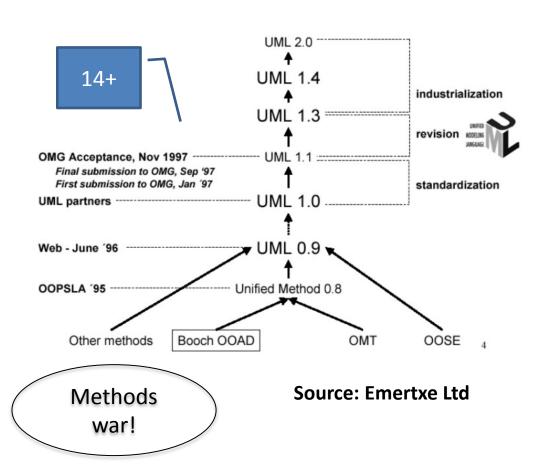
A system aspect, or system view, is a way to look at or describe a system as a whole. Each system aspect has its own associated semantic domain and can provide

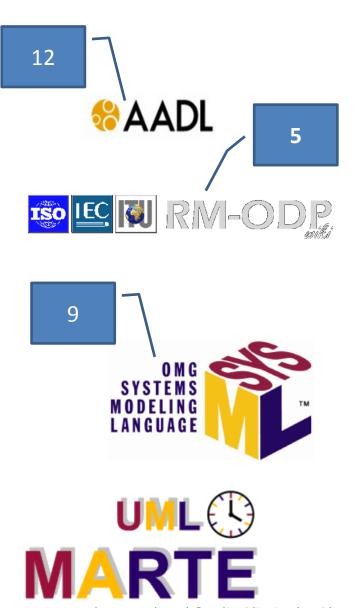
an exhaustive description of the system, but only from that particular point of view.





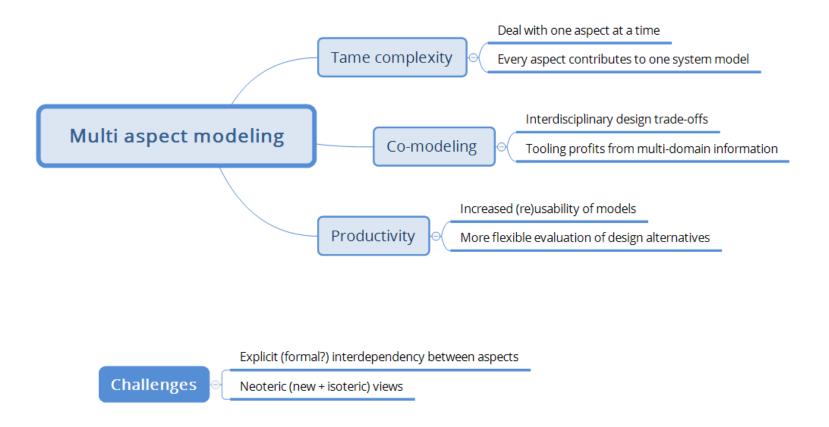
Examples





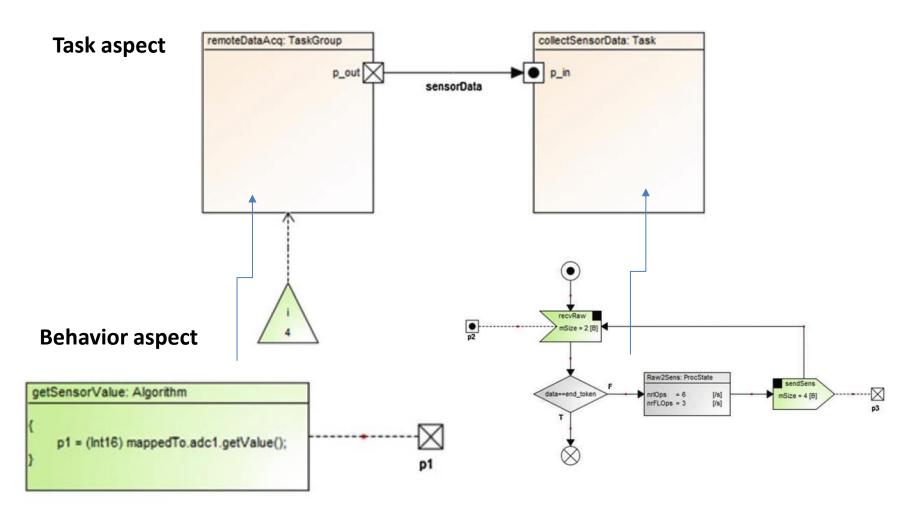


Advantages of multi-aspect modeling





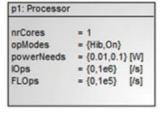
An example from CERBERO 1/3





An example from CERBERO 2/3

Physical aspect



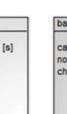
= 23

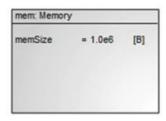
= 1.01

= none

clk1: Clock offset

driftModel

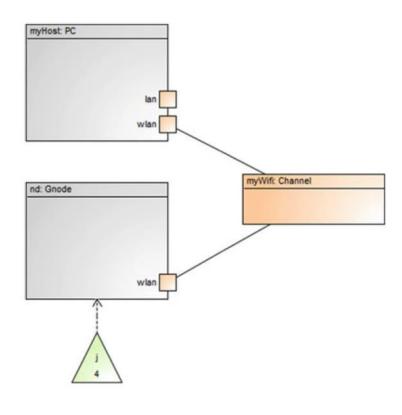




capacity	= 2.5	[Ah]
nominalVoltage	= 12	[V]
chargeModel	= none	

protocol	= Wifi	
opModes	= {Off,On}	
powerNeeds	= {0,0.05}	[W]
bandwidths	$= \{0,1e6\}$	[B/s]

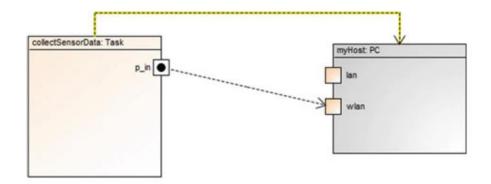
nrBits	= 12	
maxRange	= 5.0	[V]
offset	= 2	[mV]

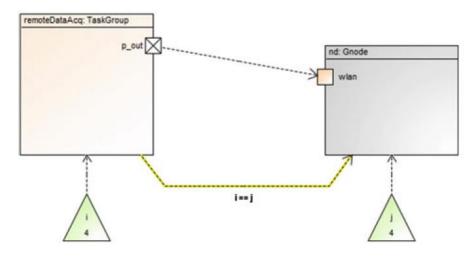




An example from CERBERO 3/3

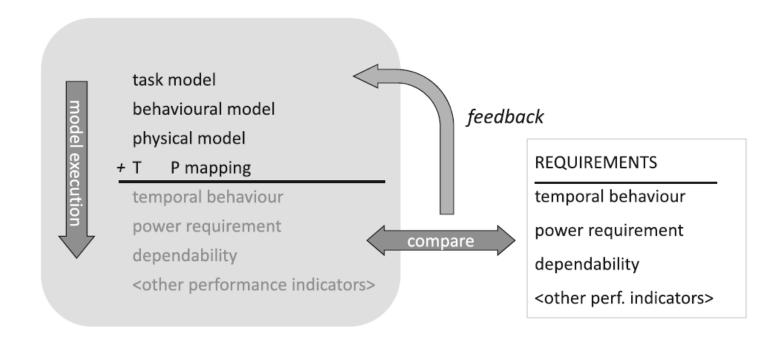
Mapping view





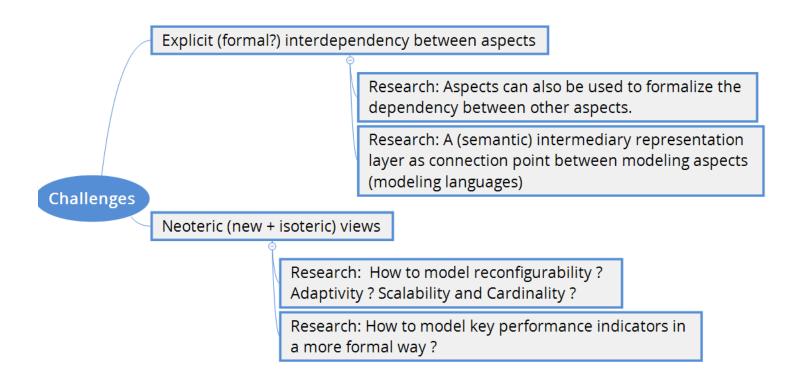


Using the models together to assess KPIs





Some CERBERO contributions (expected)



Component level > Outline

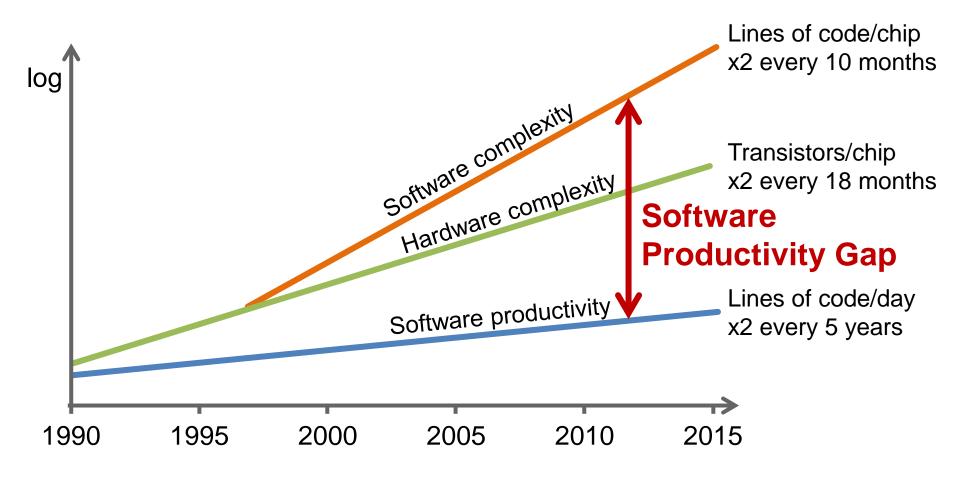


Component level SW/HW (co-)design

- 1. State-of-the-Art
- 2. Models of Computation
- 3. Models of Architecture

Component level > State of the

Need for a new HW/SW design approach!

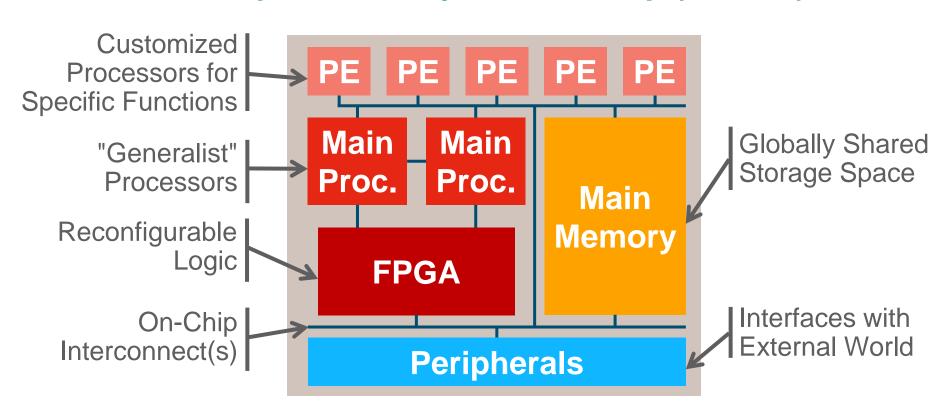




Component level > State of the

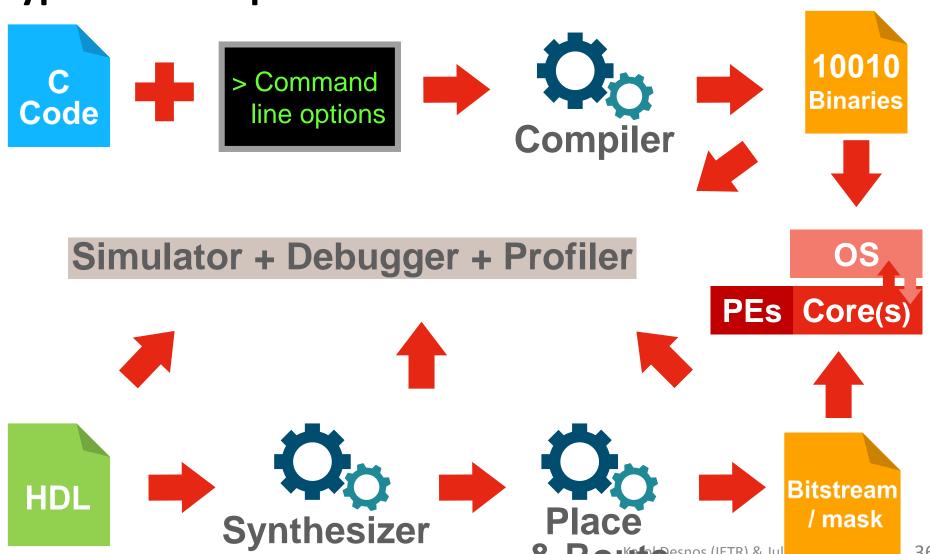
Typical HW/SW component

Heterogeneous Multiprocessor System-on-Chip (MPSoC)





Typical development flow





Component level > State of the The

C Language is:

- Good for abstracting core architecture
 - Amount of registers
 - Number of pipeline stages
 - Instruction parallelism
- Bad for expressing coarse-grain parallelism
 - Inspired by Turing Machine
 - Global state in a program



Component level > State of the The Component level > State of the Compo

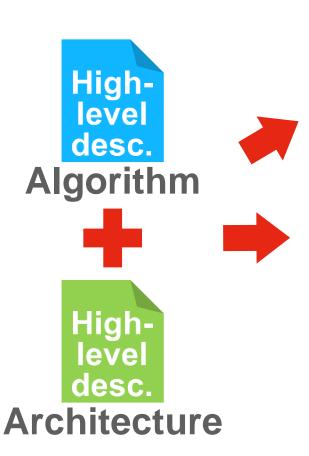
VHDL/Verilog Languages are:

- Good for abstracting
 - Transistors
 - Analog concerns (signal propagation time)
- Bad for abstracting
 - Software concerns
 - ... (more reasons in HLS and HW courses)



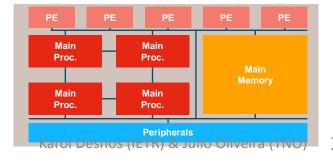
Component level > State of the

What we want?



Simulator + Debugger + Profiler





Component level > Outline



Component level SW/HW (co-)design

- 1. State-of-the-Art
- 2. Models of Computation
- 3. Models of Architecture



Model of Computation (MoC)

a.k.a. programming paradigm

Definition:

- A set of operational elements that can be composed to describe the behavior of an application.
 - → Semantics of the MoC

Objective:

- Specify implementation-independent system behavior.
- Ease specification, implementation, verification of system properties.

How:

MoCs act as the interface between computer science
 & mathematical domain.





Language

Definition:

- A set of textual/graphical symbols that can be assembled respecting a well defined grammar to specify the behavior of a program
 - → Syntax of a the language

Objective:

- Ease system description and maximize developer productivity.
- Be developer-friendly: readability, reusability, modularity, ...

How:

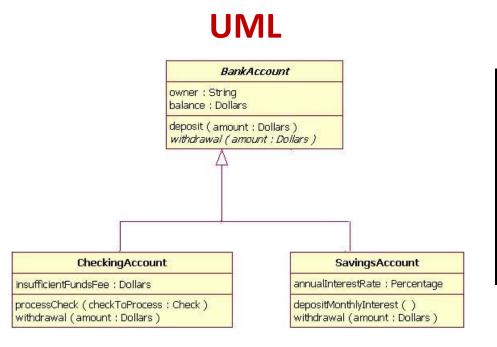
Languages are the interface between the programmer
 & the Machine (through the complier).

A Language implements one or several MoCs



MoC Semantics and Language Syntax

- UML implements object-oriented semantics
- C++/Java implements object-oriented semantics
- They share semantics but not syntax



Java

```
public class SavingsAccount
extends BankAccount {
  private int annualInterestRate;

  public void withdrawal(int v) {
    ...
  }
}
```





A few MoCs

Finite State Machine MoCs

Semantics

- States
- Transitions (possibly conditional)

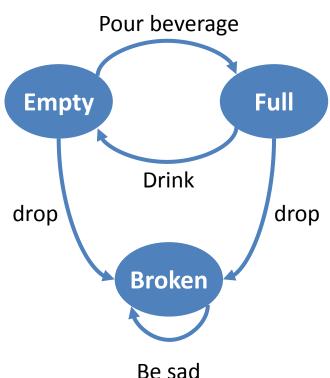
Used for

- Sequential logic
- System-level behavior
- Communication protocols

Property

Non-deterministic, sequential

Glass FSM





A few MoCs

Petri Nets

Semantics

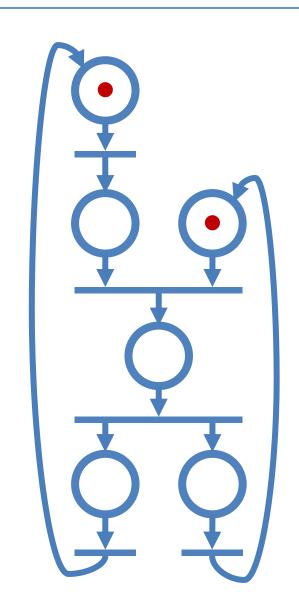
- Places
- Transitions & Arcs

Used for

- Synchronization protocols
- Parallel computations
- •

Property

- Parallelism
- Liveness, Boundedness, Reachability





A few MoCs

Discrete Event MoCs

Semantics

- Modules
- Signals
- Timed events
- Global clock

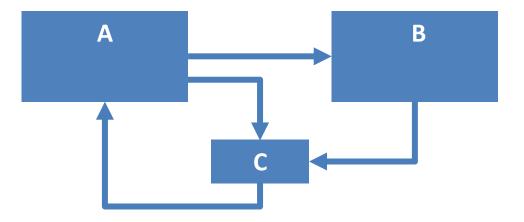
Used for

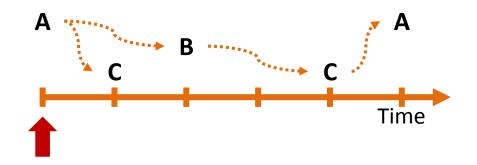
- Hardware Description
- "System" Simulation

Properties

• Timed, Non-deterministic (if badly used)

[Agrol Desnos (JETR) & Julio Oliveira (TNO)]







A few MoCs

Kahn Process Network

Semantics

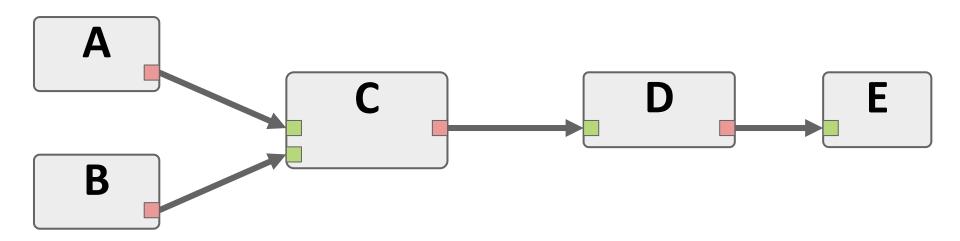
- Actors & ports
- FIFO queues

Used for

- Parallel computations
- Stream processing

Properties

- Deterministic
- Untimed





A few MoCs

Kahn Process Network (KPN)

Determinism



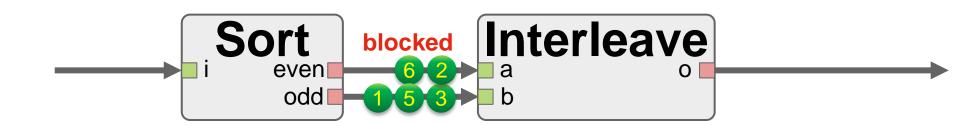
```
Process sort(in int i, out int even, out int odd) {
  int value = i.read(); // Blocking
  if( value % 2 == 0)
    even.write(value);
  else
    odd.write(value);
}
```



A few MoCs

Kahn Process Network (KPN)

Determinism



```
Process inteleave(in int a, in int b, out int o) {
   static bool = true;
   int value = (bool)? a.read() : b.read();
   bool = !bool;
   o.write(value);
}
```



A few MoCs

Dataflow Process Network (DPN)

Non-Determinism



```
Process inteleave(in int a, in int b, out int o) {
   static bool = true;
   int value = (bool)? a.read() : b.read();
   bool = !bool;
   if(no_timeout) o.write(value);
}
```



A few MoCs

Synchronous Dataflow

Semantics

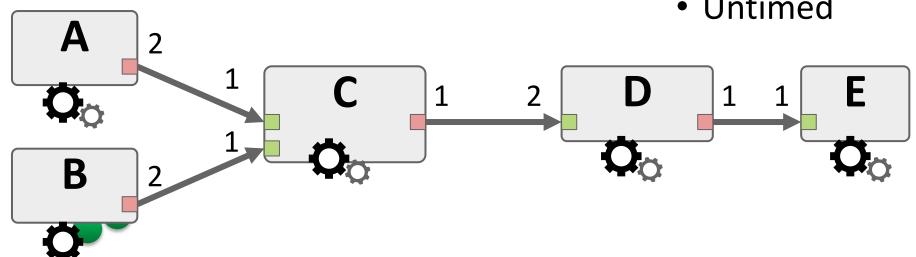
- Actors & ports
- FIFO queues

Used for

- Parallel computations
- Stream processing

Properties

- Liveness
- Boundedness
- Deterministic
- Untimed





MoC Properties are important.

You need to know them to select the MoC suiting your needs

Feature	SDF	ADF	IBSDF	DSSF	PSDF	PiSDF	SADF	SPDF	DPN	KPN
Expressivity	Low				Med.		Turing			
Hierarchical			Х	Х	Х	Х				
Compositional	Ī		X	X		X				
Reconfigurable	Ī				х	X	Х	X	X	X
Statically schedulable	Х	X	X	X						
Decidable	Х	X	X	X	(X)	(X)	Х	(X)		
Variable rates	Ī	X			х	X	Х	X	X	X
Non-determinism	Ī						Х	X	X	

SDF: Synchronous Dataflow

ADF: Affine Dataflow

IBSDF: Interface-Based Dataflow

DSSF: Deterministic SDF with Shared Fifos

PSDF: Parameterized SDF

PiSDF Parameterized and Interfaced SDF

SADF: Scenario-Aware Dataflow

SPDF: Schedulable Parametric Dataflow

DPN: Dataflow Process Network

KPN: Kahn Process Networknos (IETR) & Julio Oliveira (TNO)

Component level > Outline



Component level SW/HW (co-)design

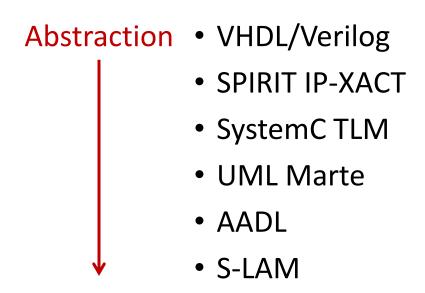
- 1. State-of-the-Art
- 2. Models of Computation
- 3. Models of Architecture



Models of Architecture

Definition:

• Formal representation of the operational semantics of networks of functional blocks describing architectures.



Source: Kienhuis, B., Deprettere, E. F., Van Der Wolf, P., & Vissers, K. A methodology to design programmable embedded systems. In Embedded processor design challenges. Springer, 2002. 54





Disclaimer:

The topic of MoA is not as extensively covered in the scientific literature/industrial tools.

Ideas presented in following slides are based on recent work by Pelcat et al.

Unfortunately, these ideas can not (yet) be considered as a globally accepted reference.



Models of Architecture

Definition:

 Formal representation of the operational semantics of networks of functional blocks describing architectures

Yes, but

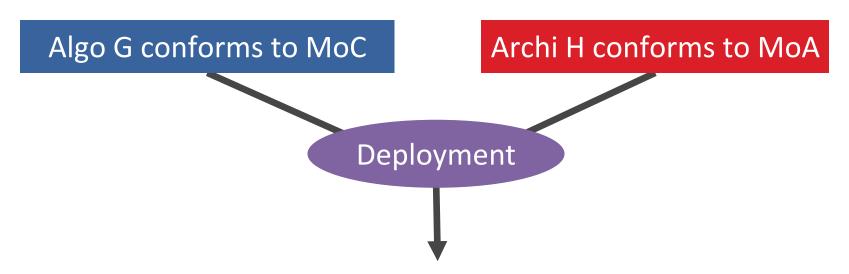
- The SDF MoC is a formal representation of the operational semantics of networks of functional blocks describing applications
- What if application = architecture?
- What if we do not want to model the architecture as a network?
- We need a more precise definition for MoAs!



Models of Architecture

Definition

 an abstract efficiency model of a system architecture that provides a unique, reproducible cost computation, when processing an application described with a specified MoC.



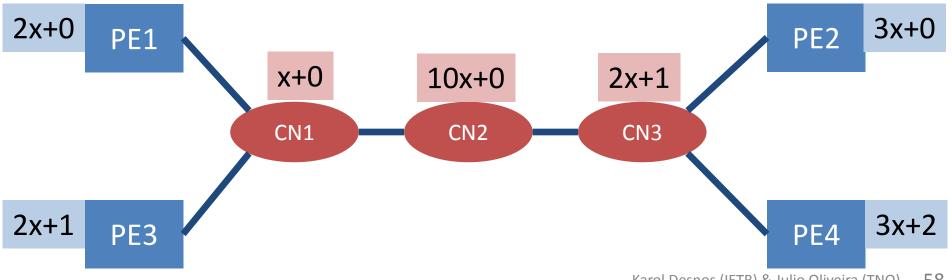
One and always the same performance number



LSLA MoA Example

Linear System Level Architecture (LSLA)

- A Model of Architecture
- Computing additive costs from application activity
- That can be used, for instance, to predict energy

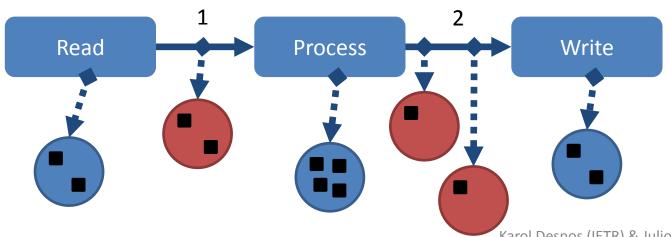




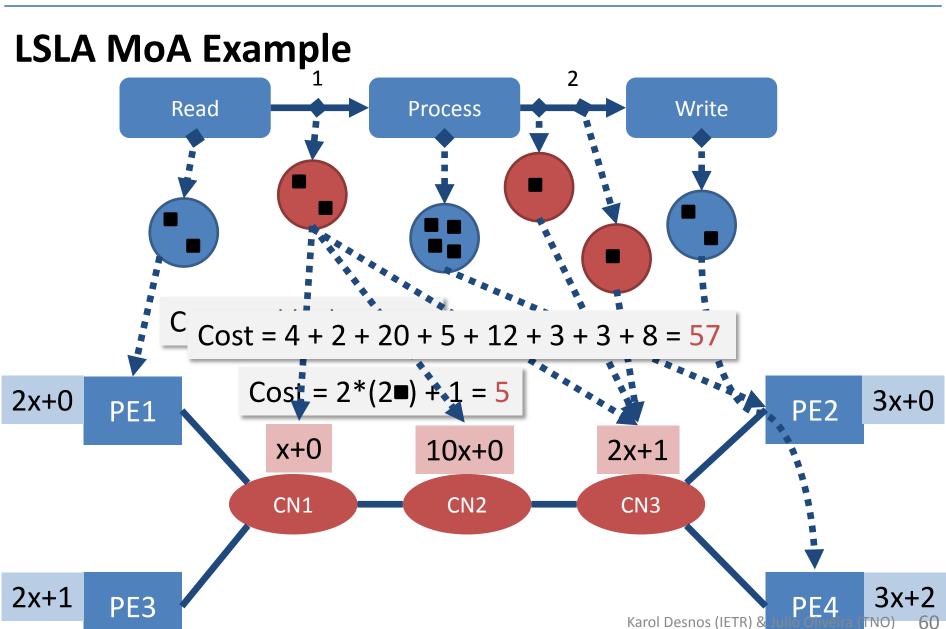
LSLA MoA Example

Application Activity for cost computation

- AA is the amount of effort to execute an application
- From the MoC, we derive
 - processing and communication tokens
- (e.g. tasks and messages)
 - processing and communication quanta
 (e.g. cycles and Bytes)





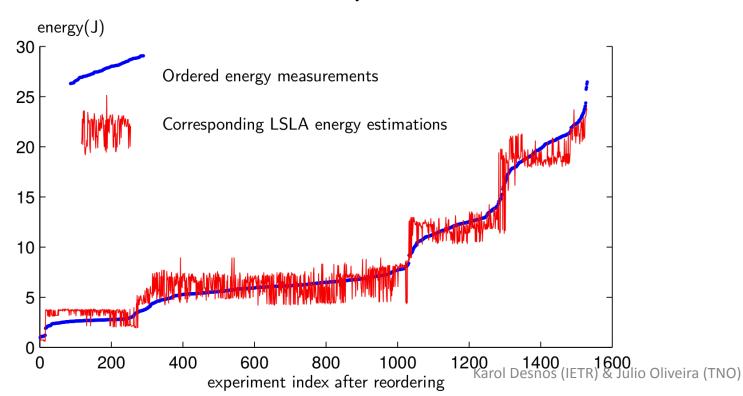




LSLA MoA example

Experiments

- On an ARM big LITTLE architecture
- Running a stereo matching application
- A simple LSLA reaches 85% of fidelity



Conclusion



Models

- offer various levels of abstraction for designing system-of-systems, system, SW and HW components
- are backed by mathematical models, providing a base for verification of system properties
- are based on semantics can be translated into actual implementation. (cf. next lecture)