System-Level HW/SW Co-Design Methodology for Real-Time and Mixed Criticality Applications

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Mixed-Criticality Embedded Systems

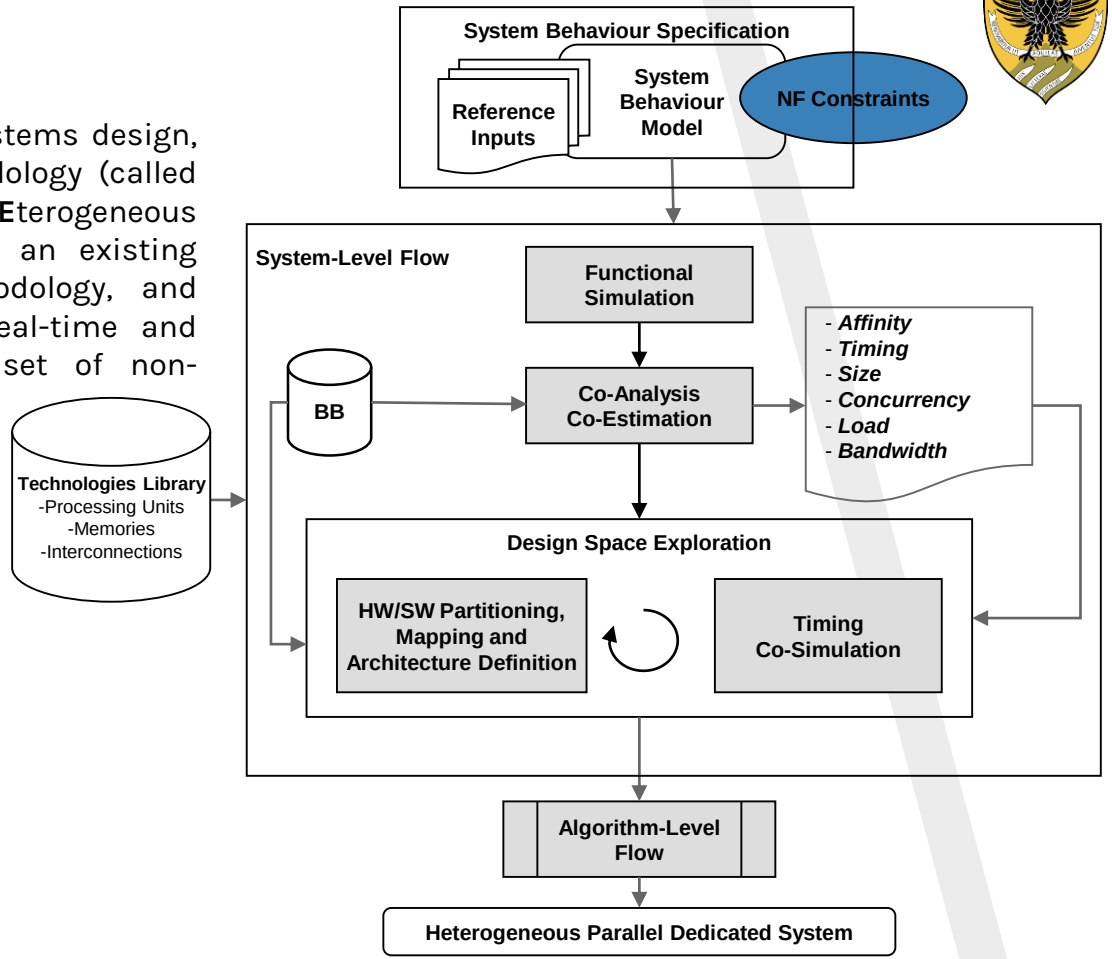
- The growing complexity of embedded digital systems based on modern System-on-Chip (SoC) adopting explicit heterogeneous parallel architectures has radically changed the common design methodologies.

- HW/SW co-design methodologies are of renovated relevance

- A growing trend in embedded systems domain is the development of mixed-criticality systems where multiple embedded applications with different levels of criticality are executed on a shared hardware platform (i.e. Mixed-Criticality Embedded Systems)

Goals

- In the context of real-time embedded systems design, this work starts from a specific methodology (called **HEPSYCODE**: HW/SW **CO-DE**sign of **HE**terogeneous **P**arallel Dedicated **SY**stems), based on an existing System-Level HW/SW Co-Design methodology, and introduces the possibility to specify real-time and mixed-criticality requirements in the set of non-functional ones



Hepsycode

www.hepsycode.com

MCS Classification

Separation technique:

- SW separation: scheduling policy, partitioning with HVP, NoC
- HW separation: one task per core, one task on HW ad hoc (DSP, FPGA), spatial partitioning with HVP, NoC

➢ **HW:**

- Temporal isolation: Scheduling HW
- Spatial isolation: separated Task on dedicated components

➢ **Single processor:**

- Temporal isolation: Scheduling policy with SO, RTOS, or HVP
- Spatial isolation : MMU, MPU, HVP Partitioning

➢ **Multi-processor (MIMD)**

- Architecture: shared memory systems, UMA (SMP), NUMA, distributed systems, NoC
- Temporal isolation : Scheduling policy con SO, RTOS, or HVP
- Spatial isolation : MMU, MPU, HVP partitioning

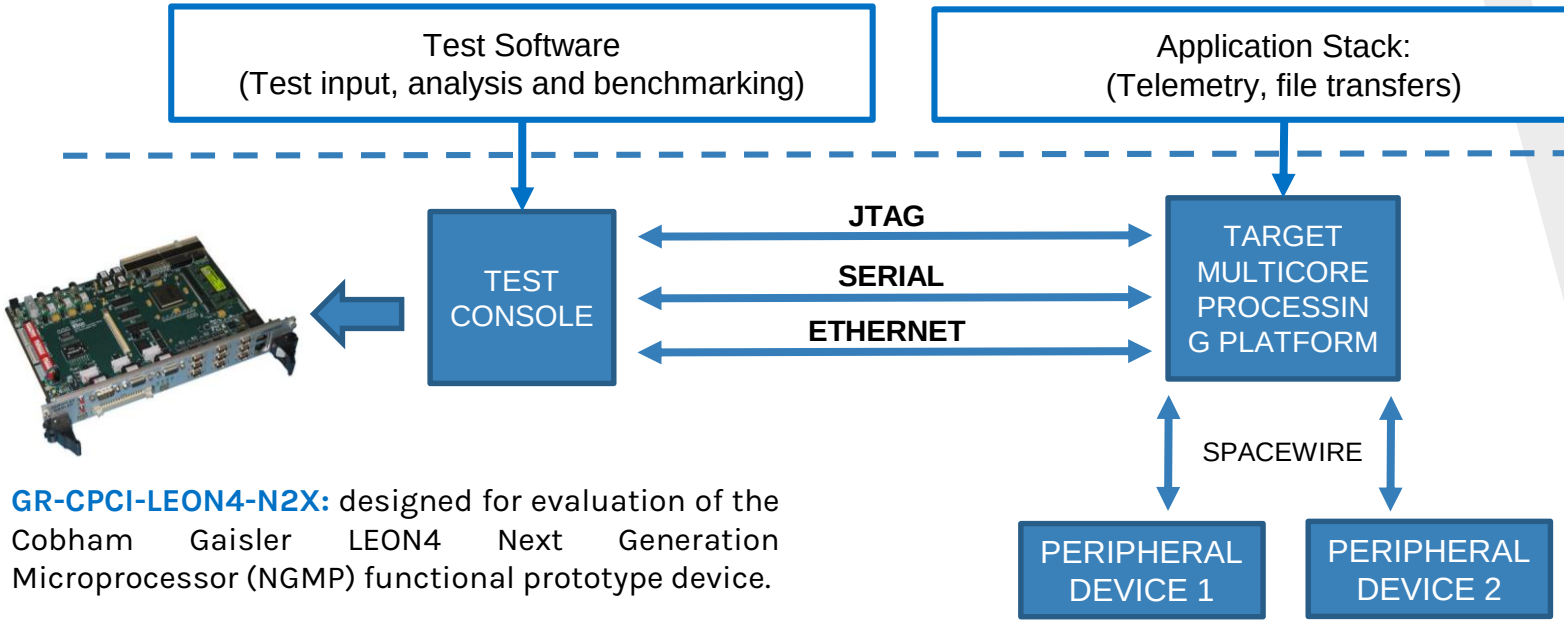
Tecnologies:

- HW: DSP, FPGA, HW ad hoc, Processor
- SW: OS, RTOS, HVP, Bare-metal
- PROCESSORI: LEON3, ARM, MICROBLAZE
- HVP: PikeOS, Xtratum, Xen
- RTOS: eCos, RTEMS, FreeRTOS, Threadx, VxWorks, Erica
- OS: Linux

Separation Technique	HW	Single core	Multi-core
Spatial	0-level scheduling [10]	0-level scheduling [11][16]	0-level scheduling [15][16]
		1-level scheduling [2][5][10][13][16]	1-level scheduling [4][9][15][16]
		2-level scheduling [6][11]	2-level scheduling [3][4][6][7] [8] [9][14]
Temporal	0-level scheduling [10]	0-level scheduling [11][16]	0-level scheduling [15][16]
		1-level scheduling [1][2][10][13] [16]	1-level scheduling [4][9][12][15][16]
		2-level scheduling [6][11]	2-level scheduling [1][4][6][7] [8] [9][14]

Multi-core Implementation

Univaq EMC² UC - Satellite Demo Platform (Hardware and Software) [8]



GR-CPCI-LEON4-N2X: designed for evaluation of the Cobham Gaisler LEON4 Next Generation Microprocessor (NGMP) functional prototype device.

Processor: Quad-Core 32-bit LEON4 SPARC V8 processor with MMU, IOMMU

XtratuM

pikeOS

- Migrate a typical aerospace application over a modern multicore platform
- Benchmarking hypervisors
- Compare different virtualization solutions

F. Federici, V. Muttillo, L. Pomante, G. Valente, D. Andreetti, D. Pascucci,: "Implementing mixed-critical applications on next generation multicore aerospace platforms", CPS Week 2016, EMC² Summit, Vienna, Austria

Design Space Exploration

- Main issues:
  - **Extension of the DSE methodology** for a better management of timing requirements in order to consider also classical RT ones
  - **Analysis of existing HW/SW technologies to** support **mixed-criticality management** (with focus on **hypervisors** technologies) to be exploited in the second-step of the DSE methodology
  - Extension of the **system-level co-simulation approach** to consider also two-levels scheduling policies typically introduced by hypervisors technologies
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AQUAS SAFETY SECURITY PERFORMANCE

MegaM@Rt²

THANKS!

Any questions?